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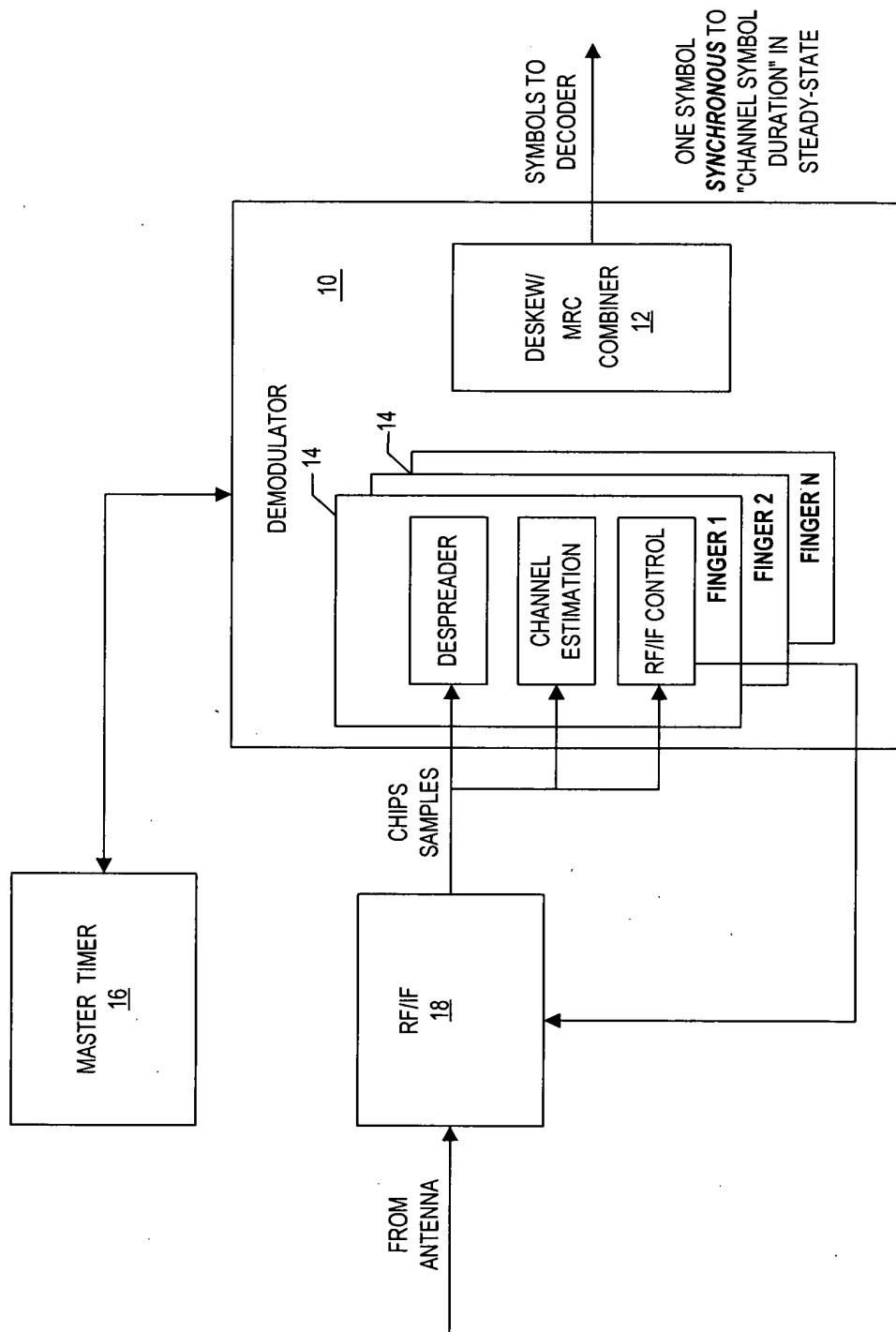
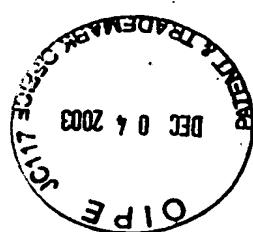


FIG. 1
PRIOR ART



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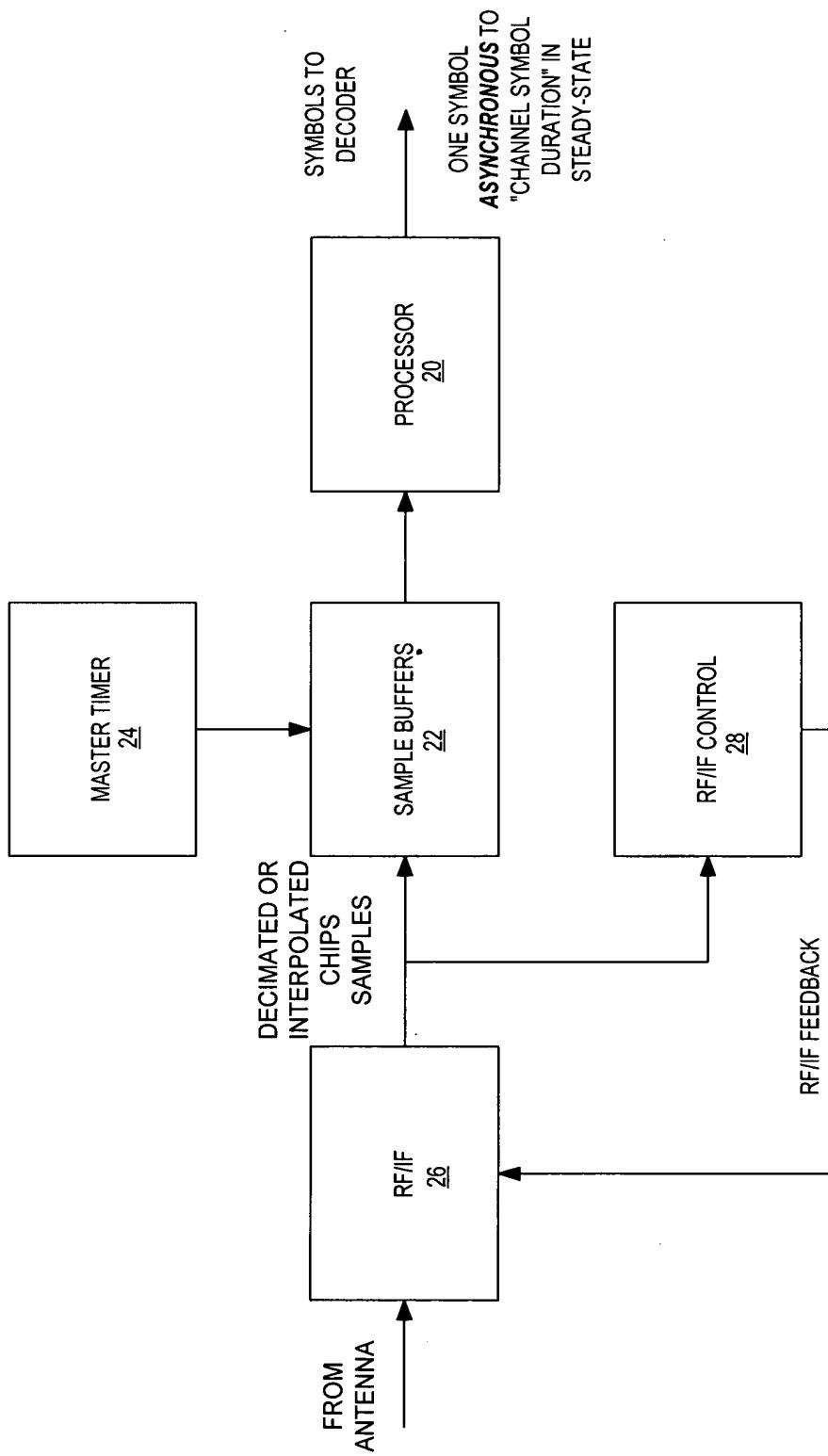
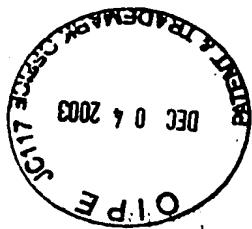


FIG. 2



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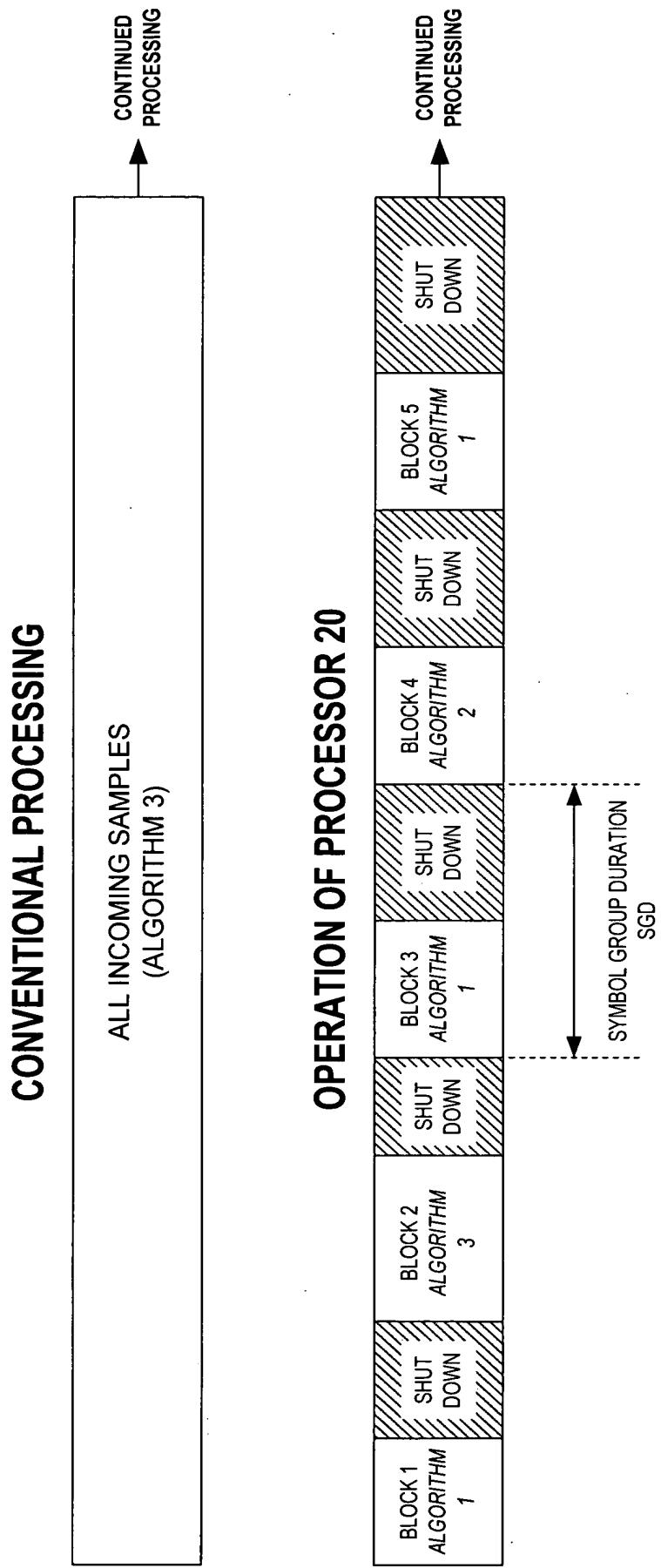


FIG. 3



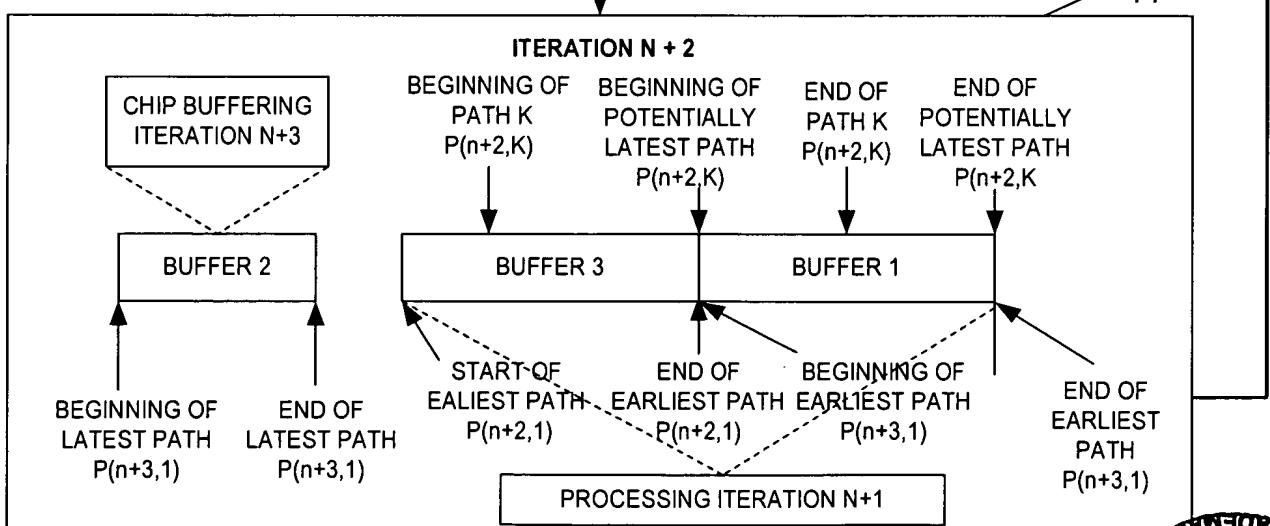
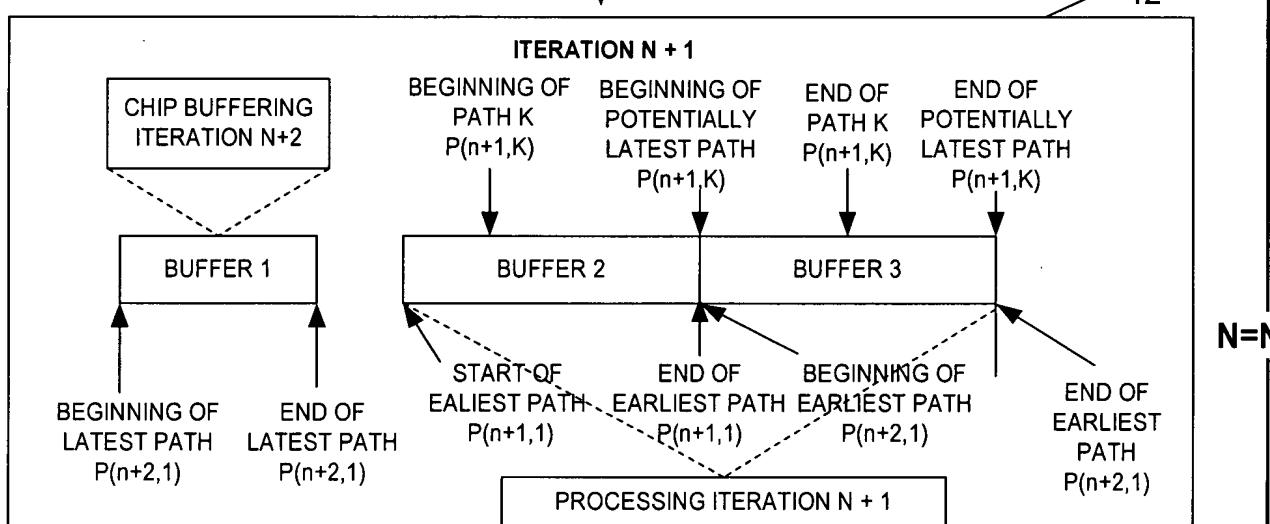
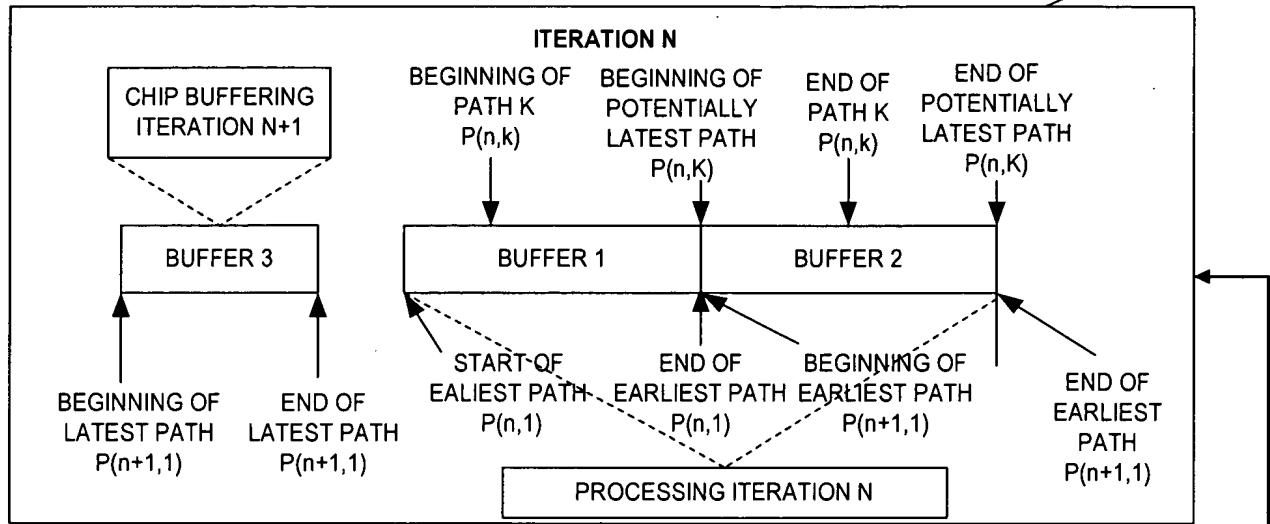
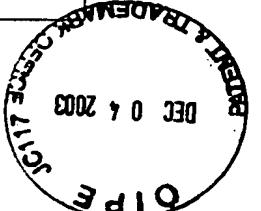


FIG. 4



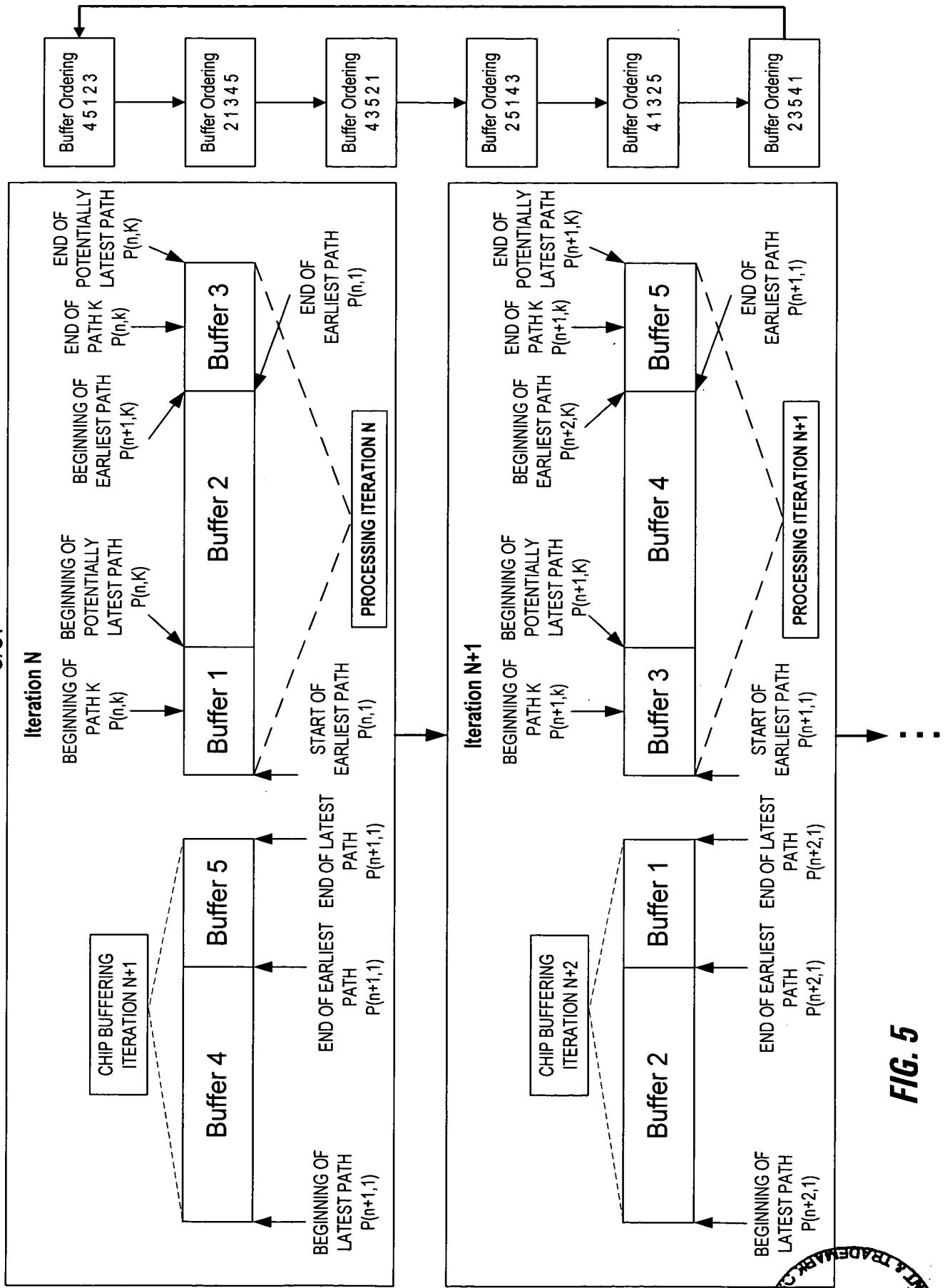
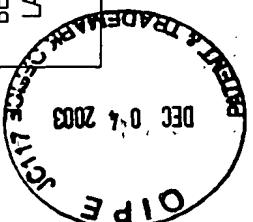
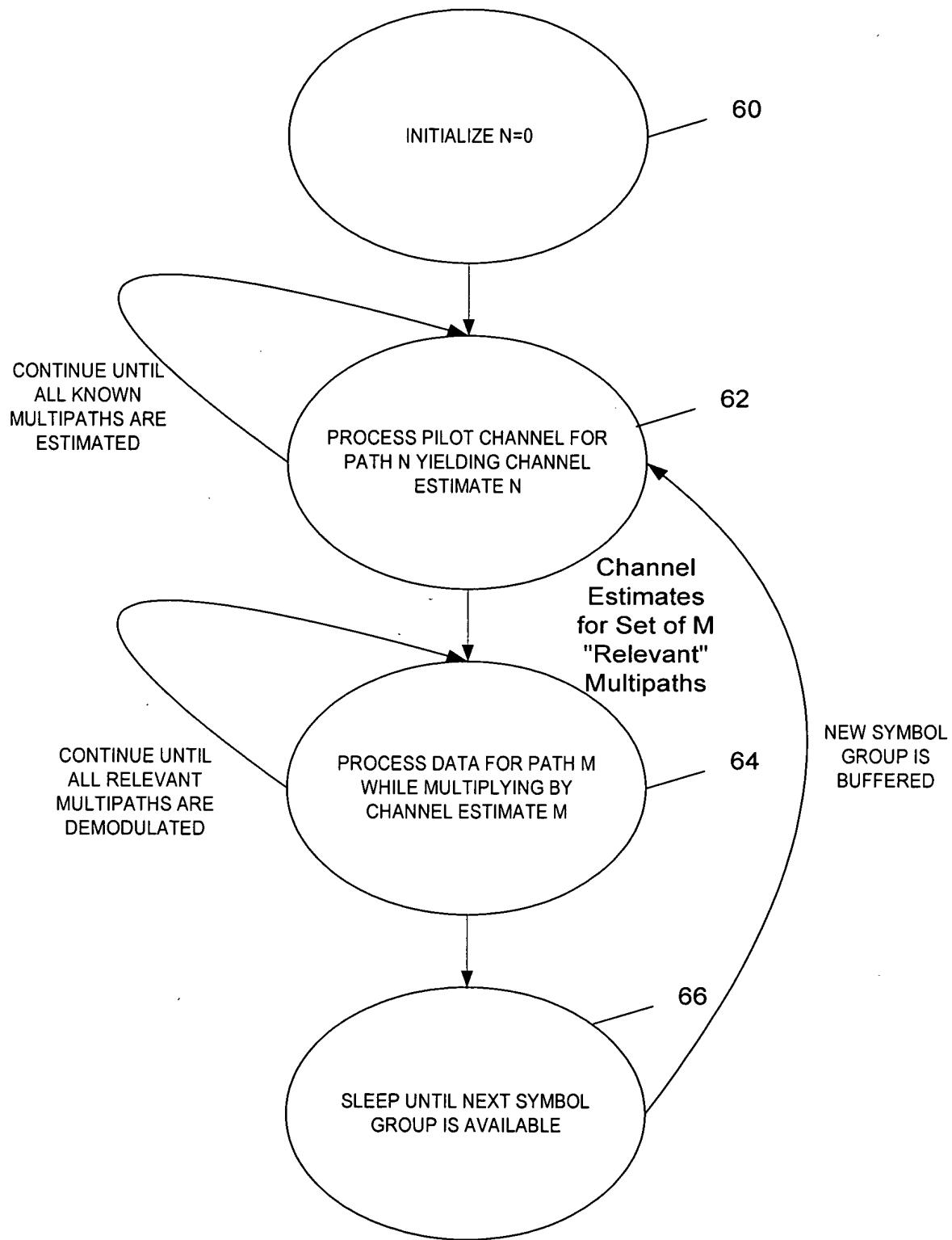
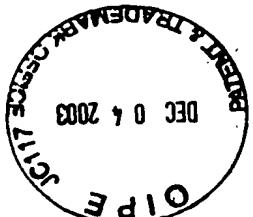


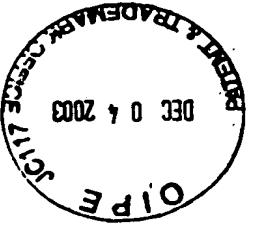
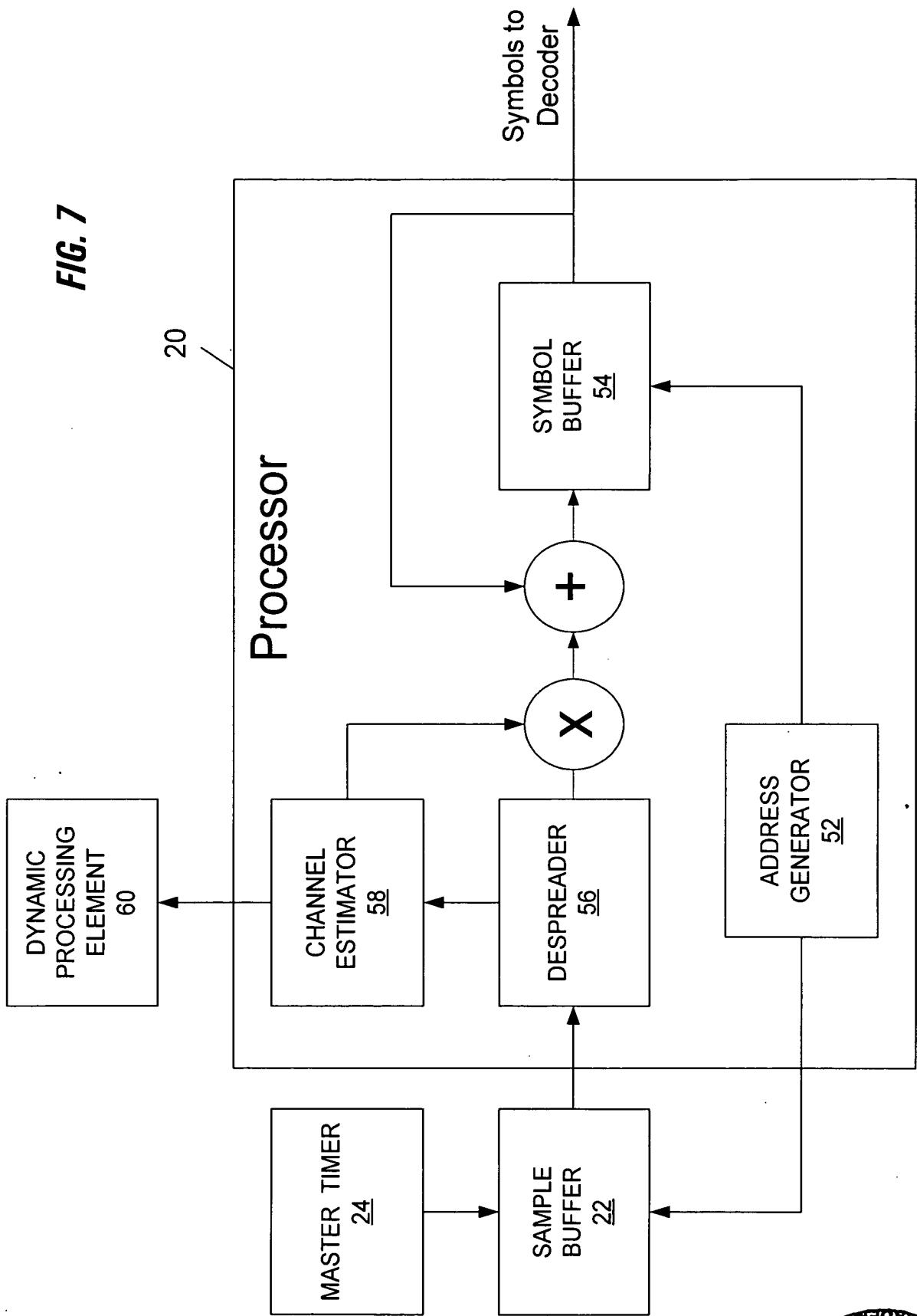
FIG. 5



**FIG. 6**

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FIG. 7



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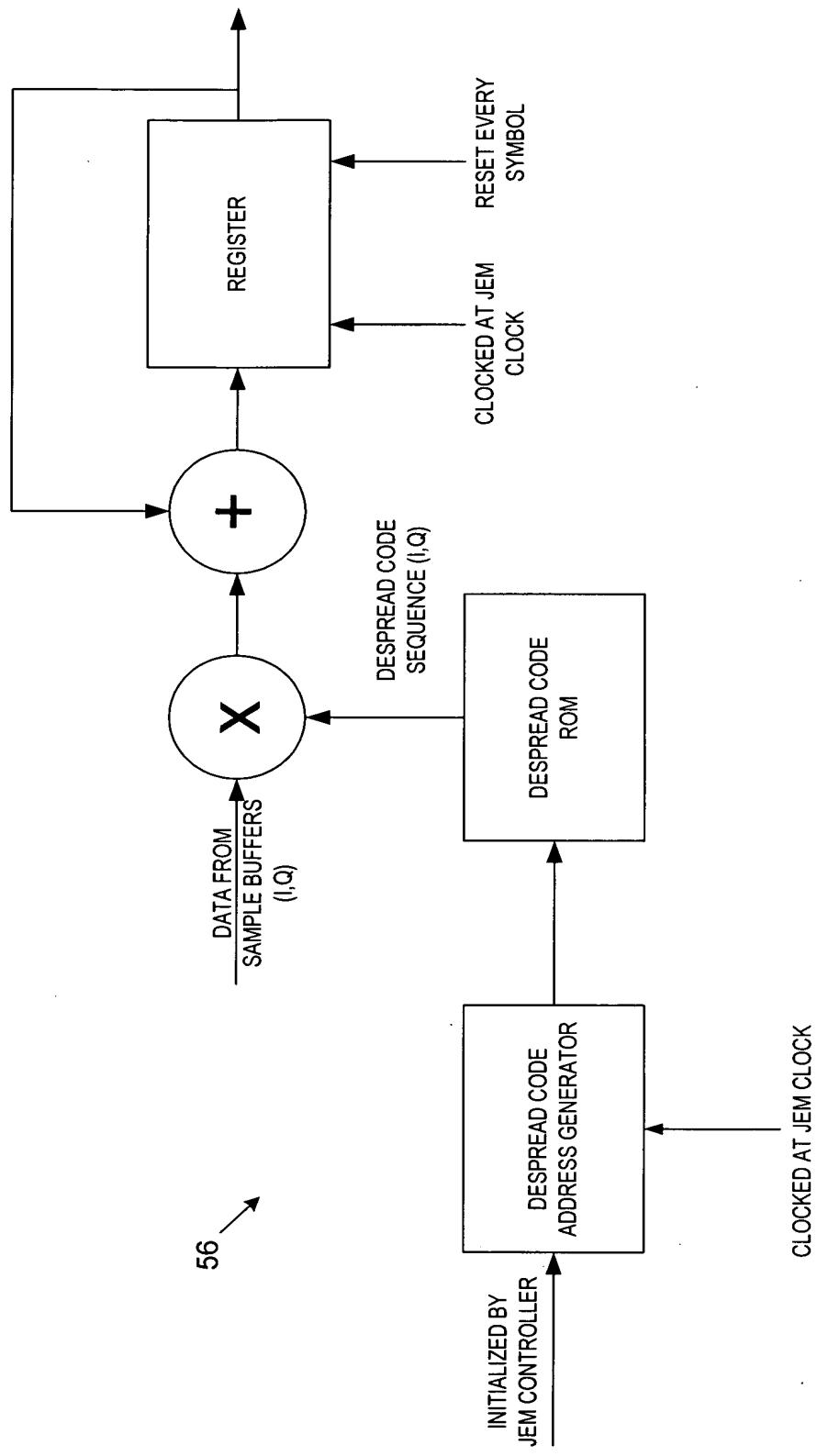
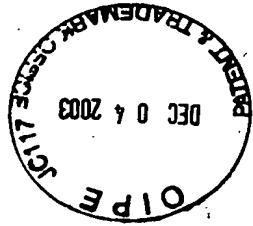


FIG. 8





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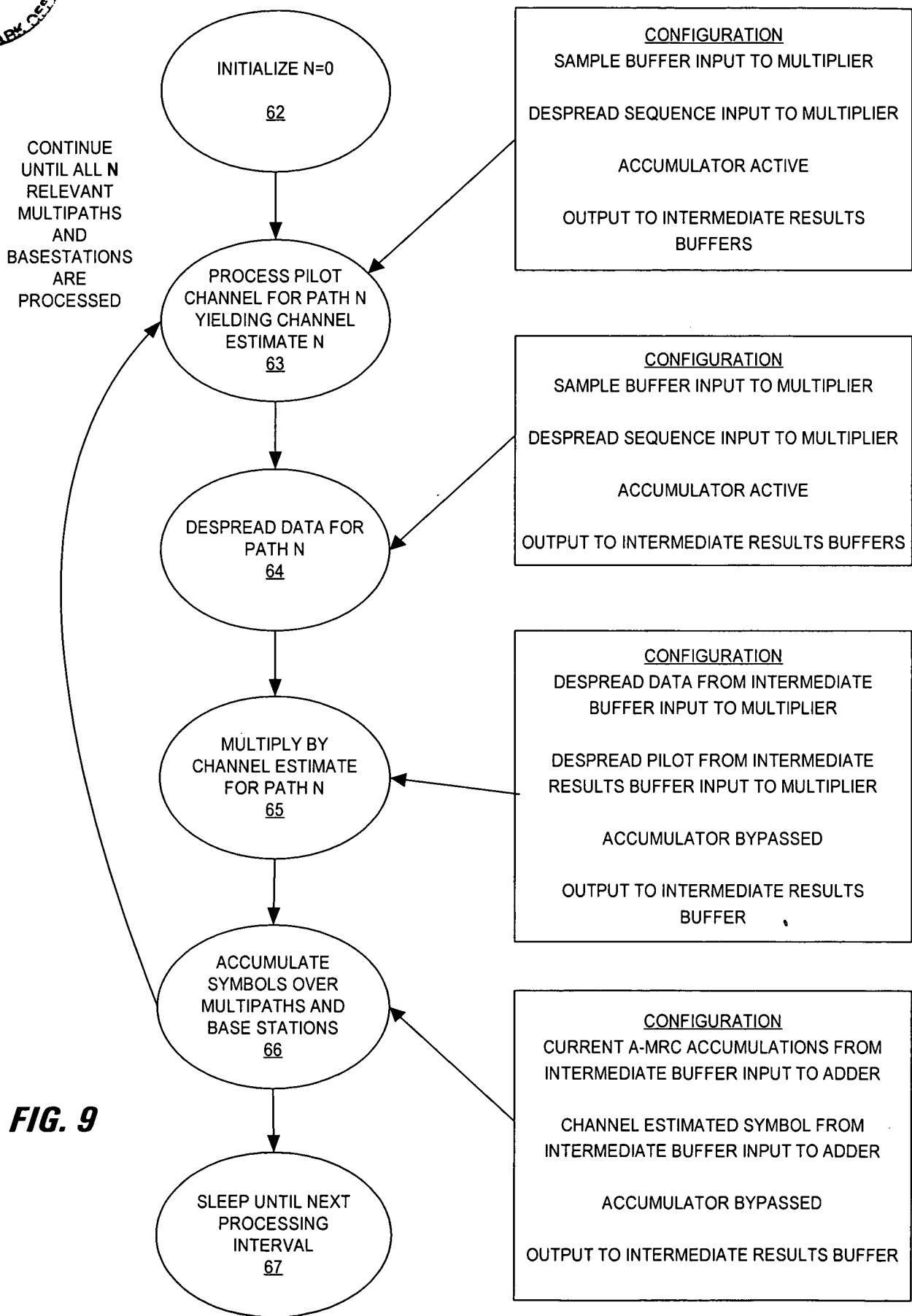


FIG. 10

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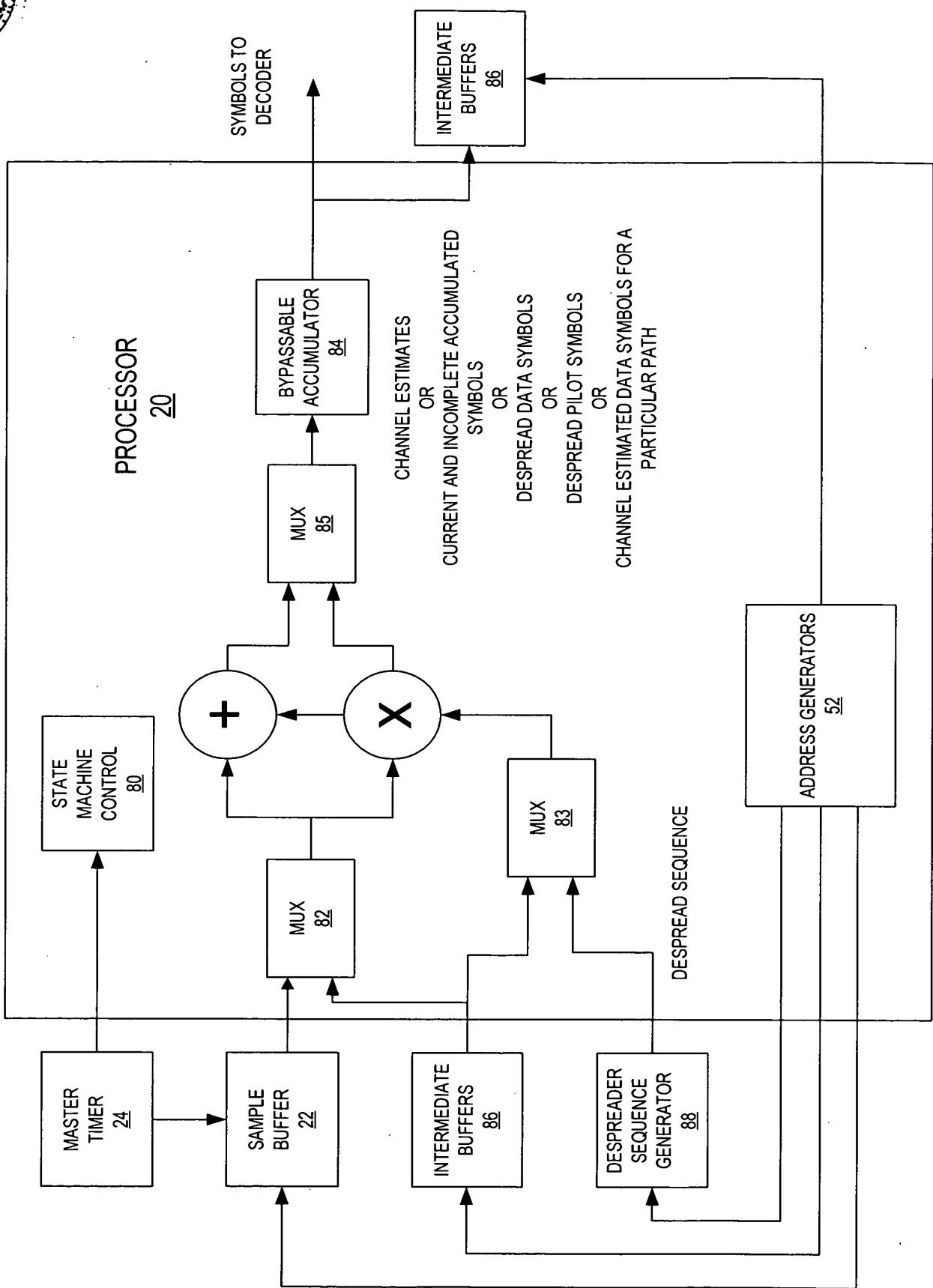




FIG. 11
PRIOR ART

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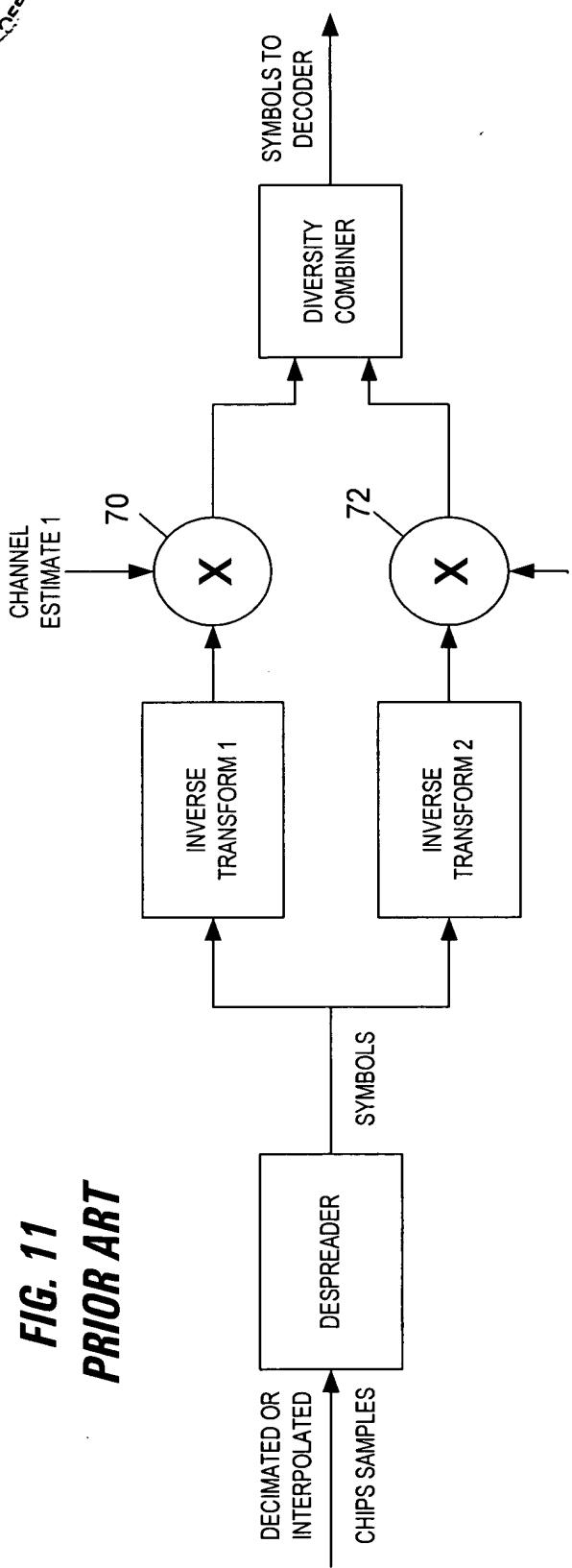
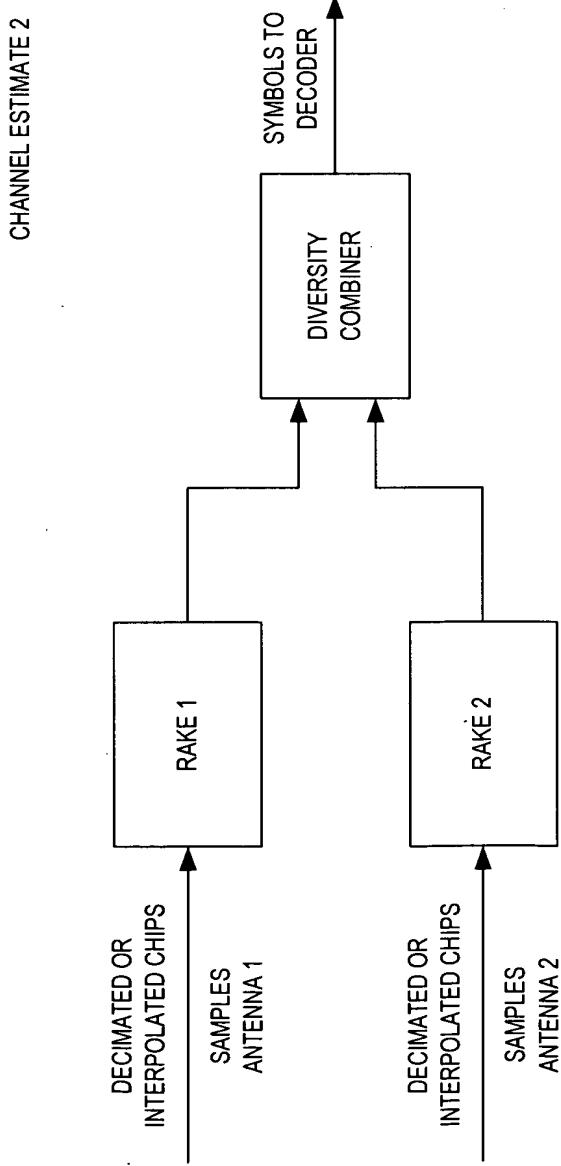


FIG. 12
PRIOR ART





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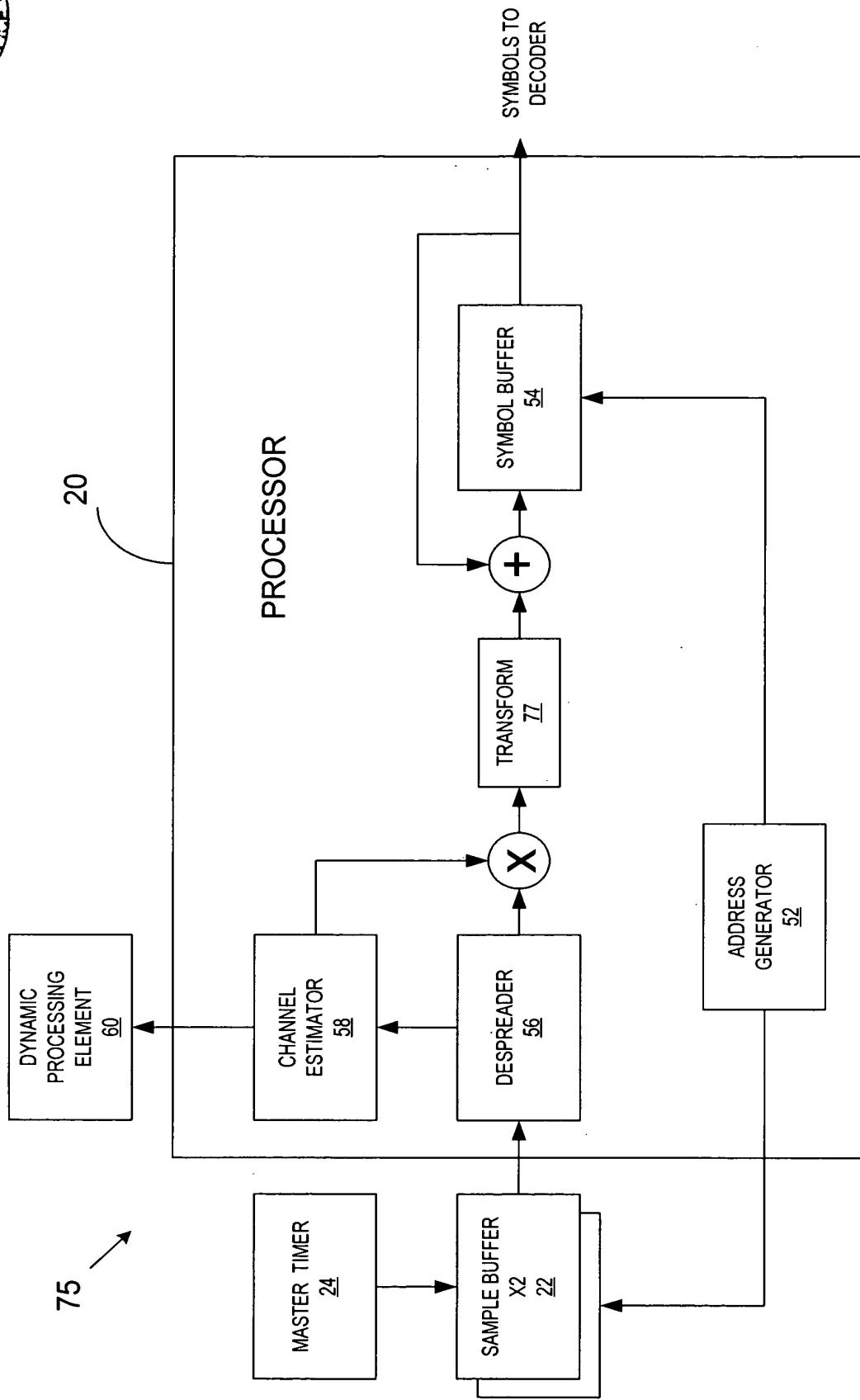


FIG. 13



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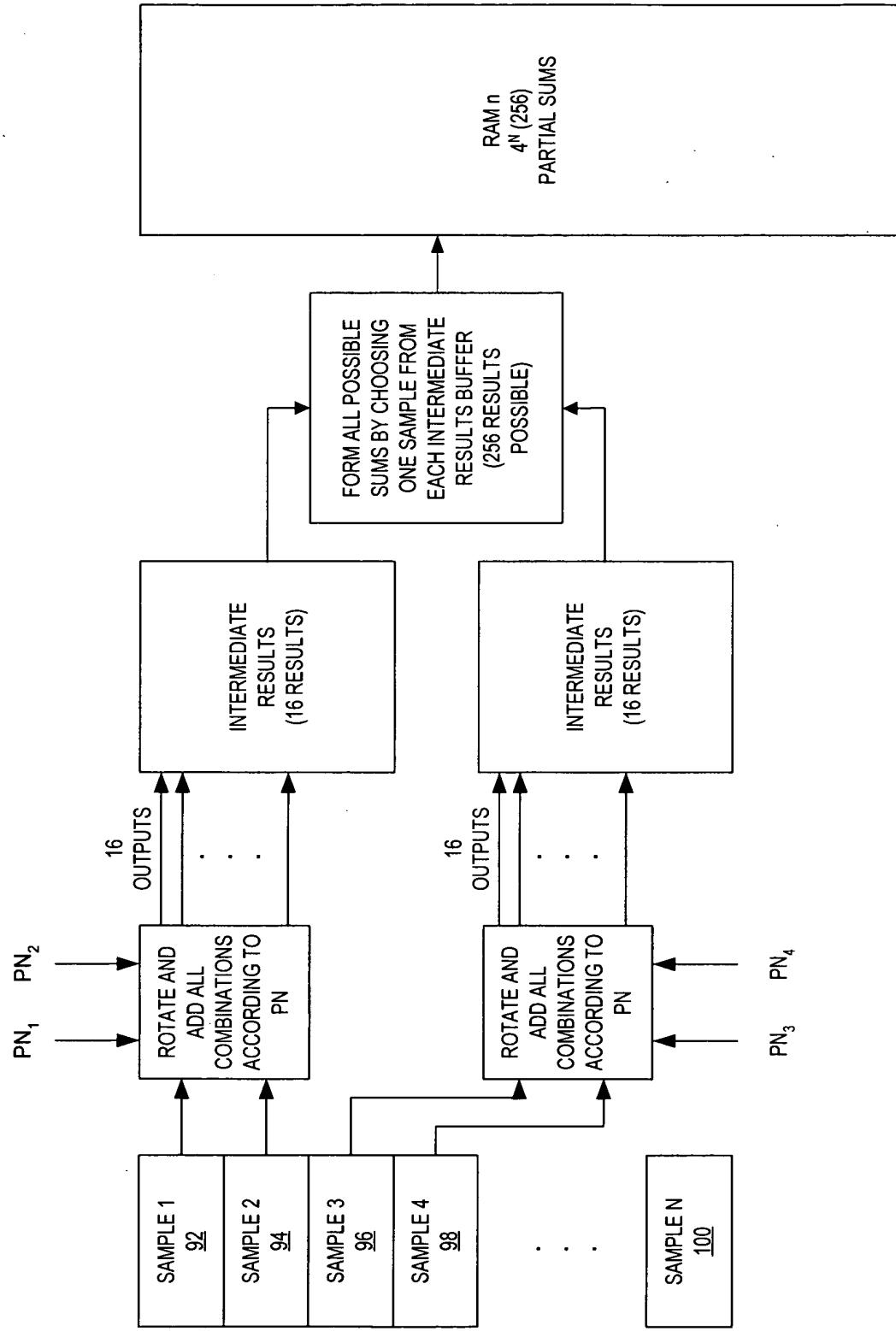


FIG. 14



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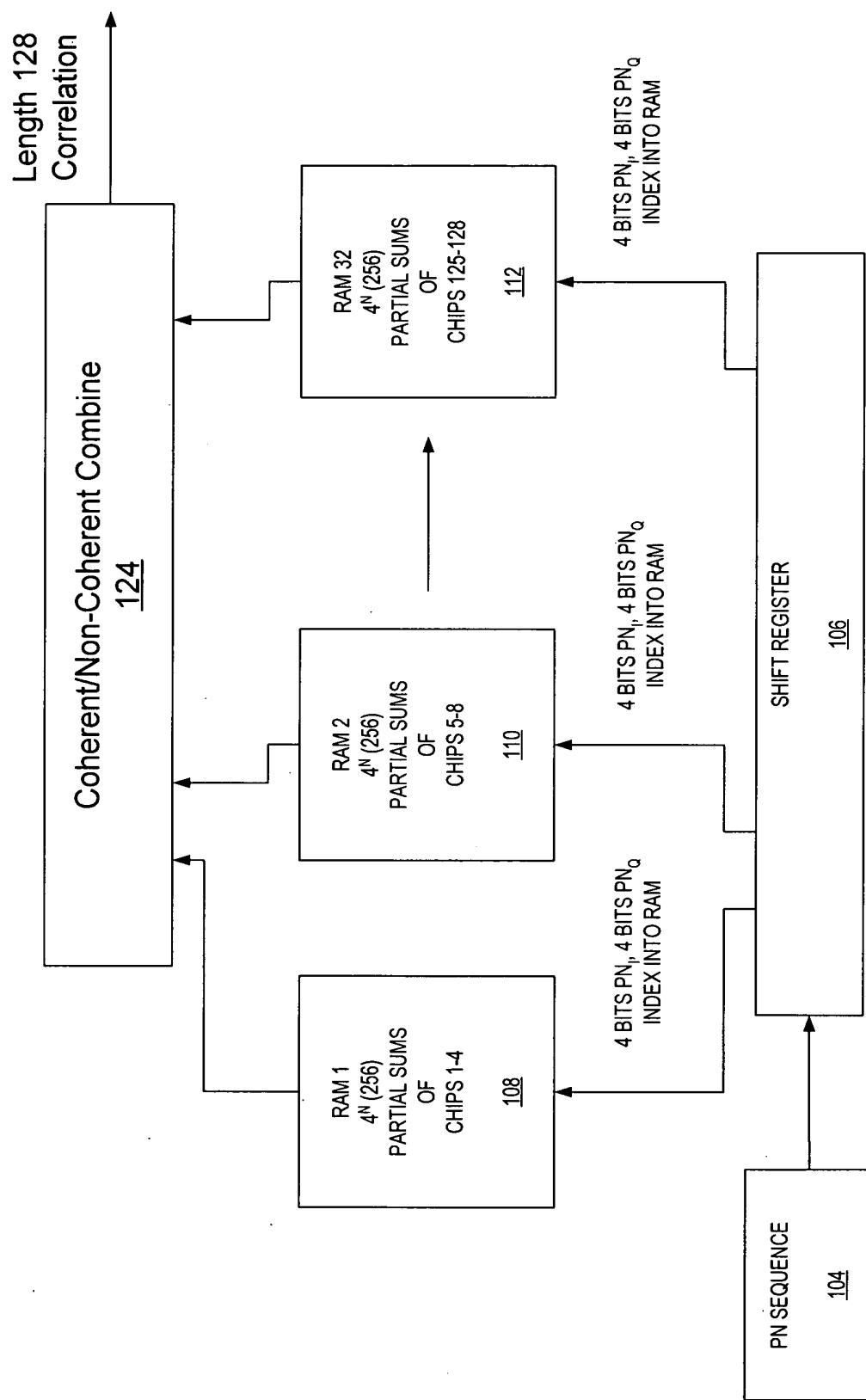


FIG. 15

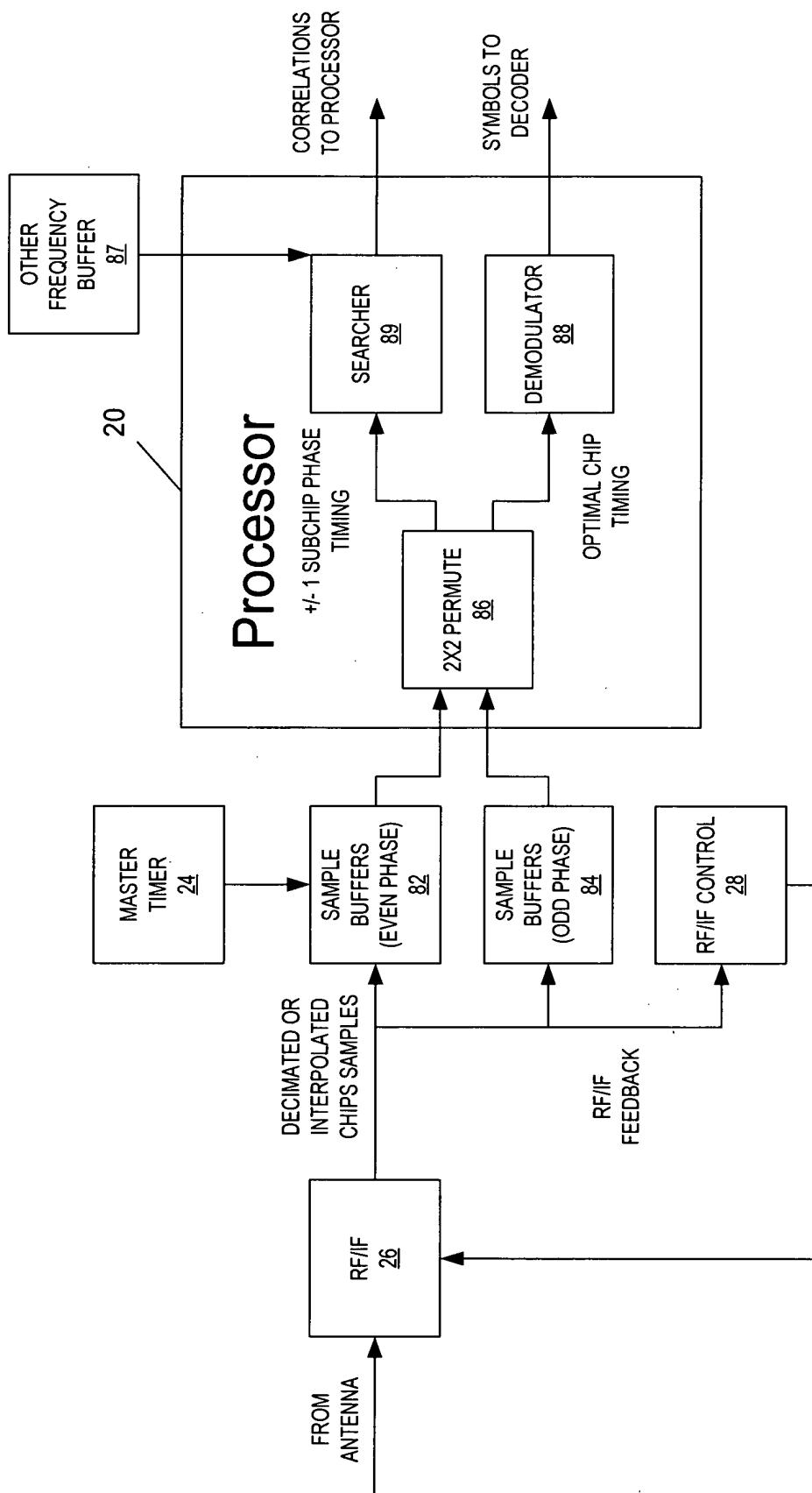
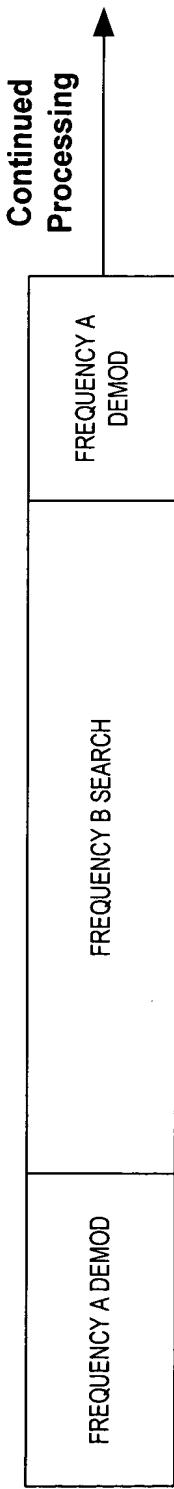


FIG. 16



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CONVENTIONAL PROCESSING



MULTI-FREQUENCY PROCESSING

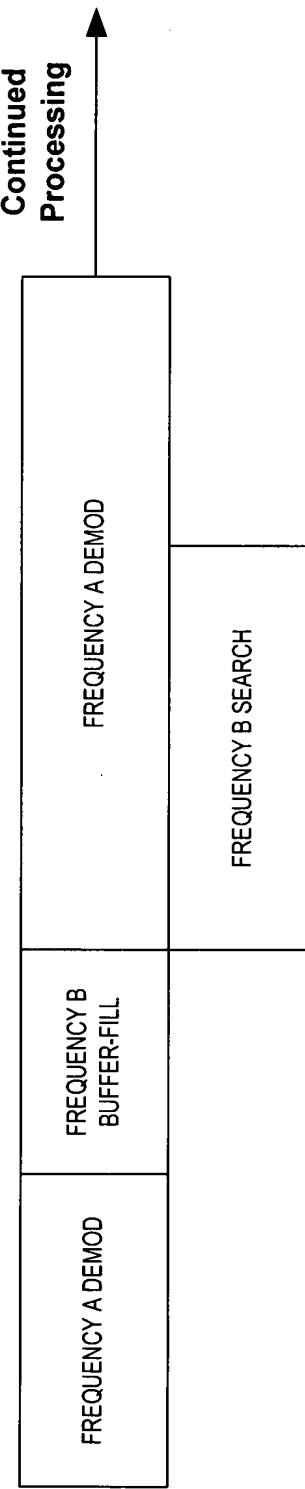


FIG. 17

O I P E
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$$R = 4 \left(\frac{E_c}{N_o} \right) \left[\frac{1}{\sqrt{E_c}} \right]$$

Received Chip, r_n



Convergent Searcher

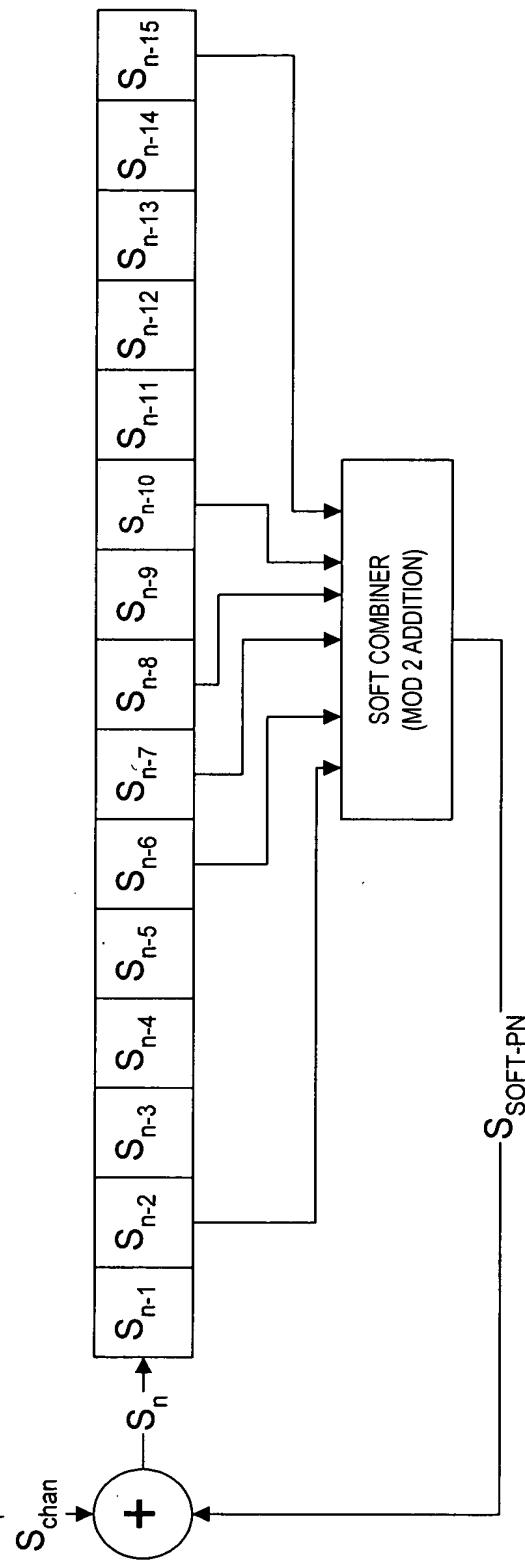


FIG. 18



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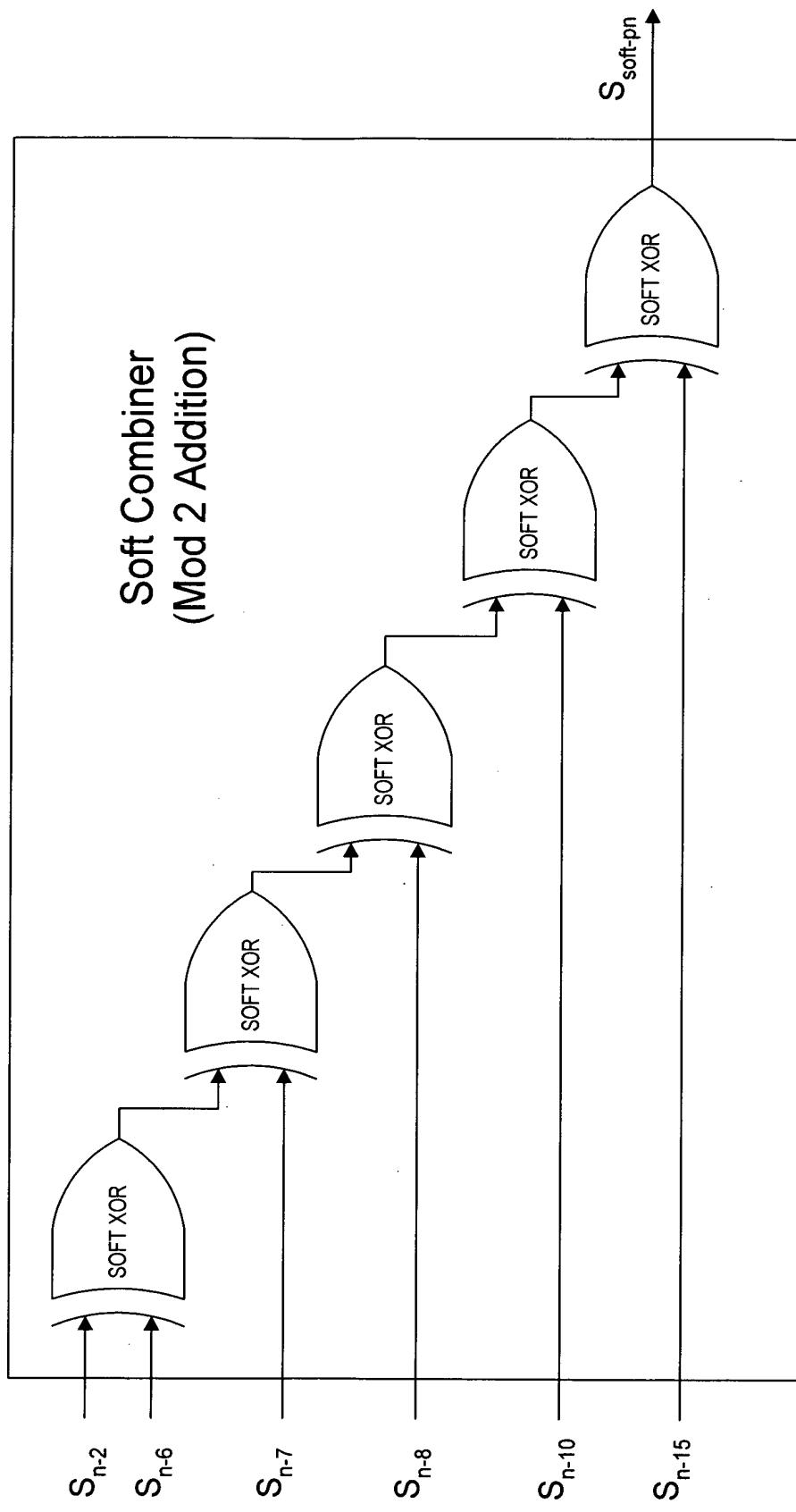


FIG. 19



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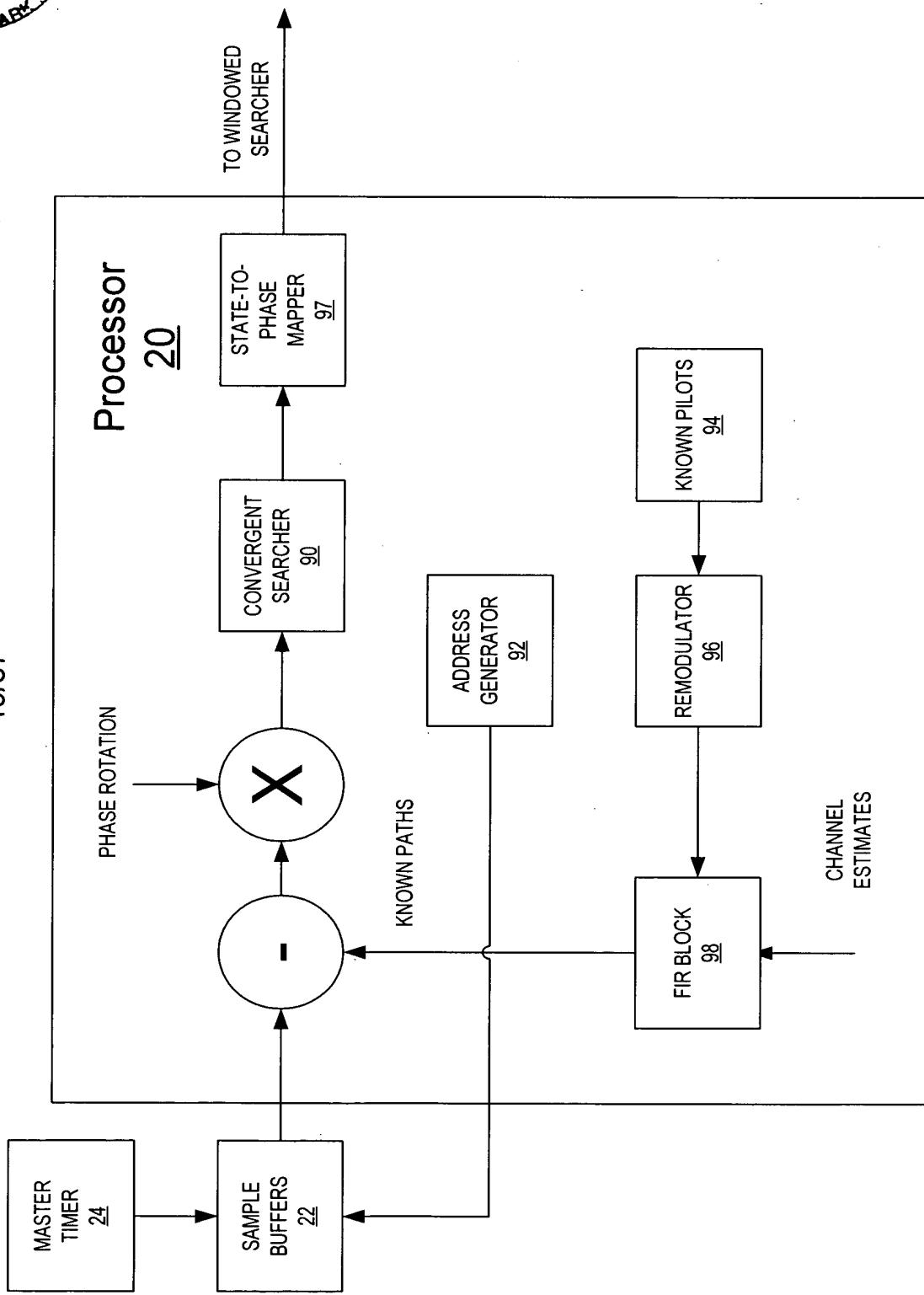


FIG. 20



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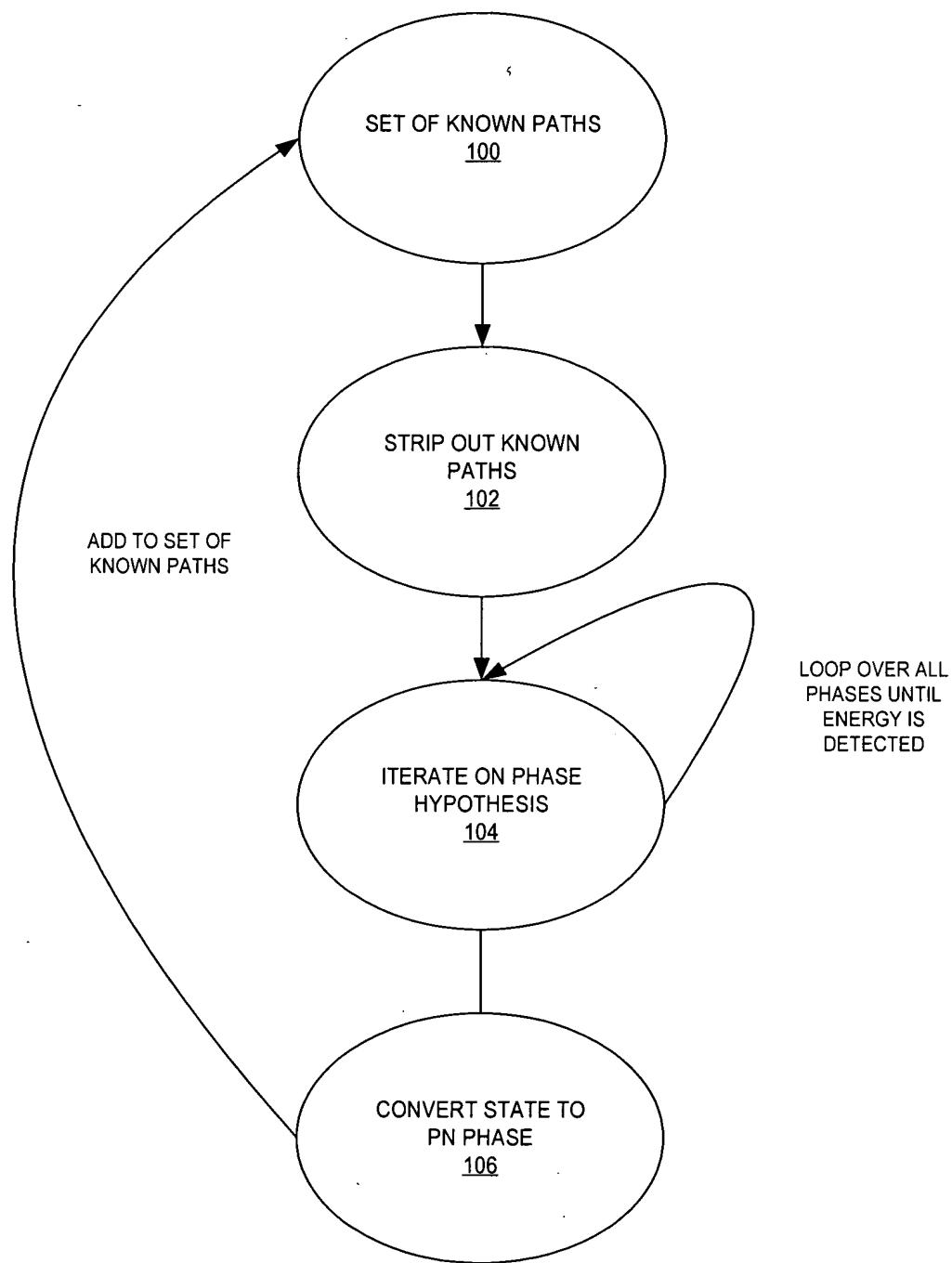


FIG. 21

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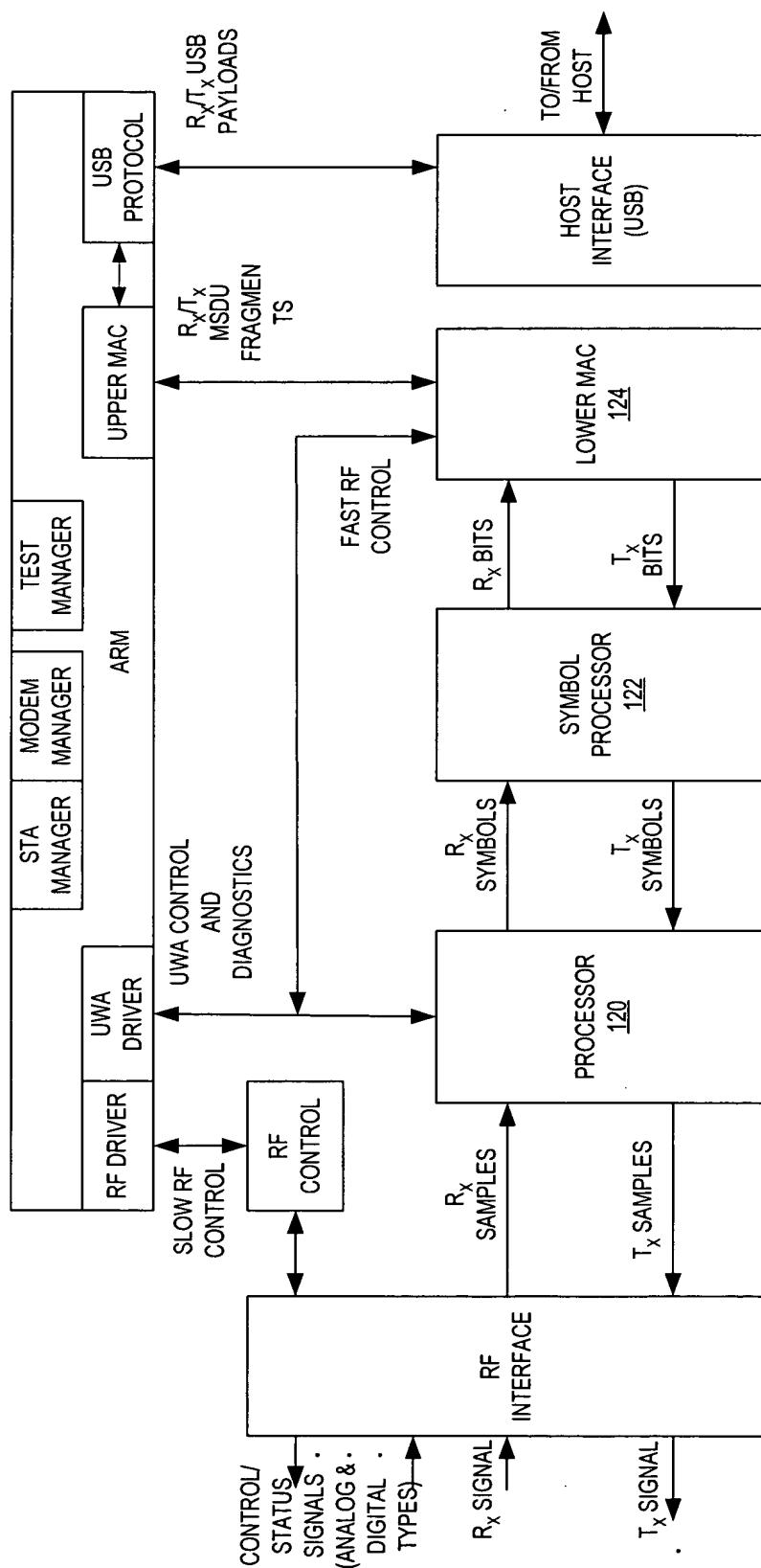


FIG. 22



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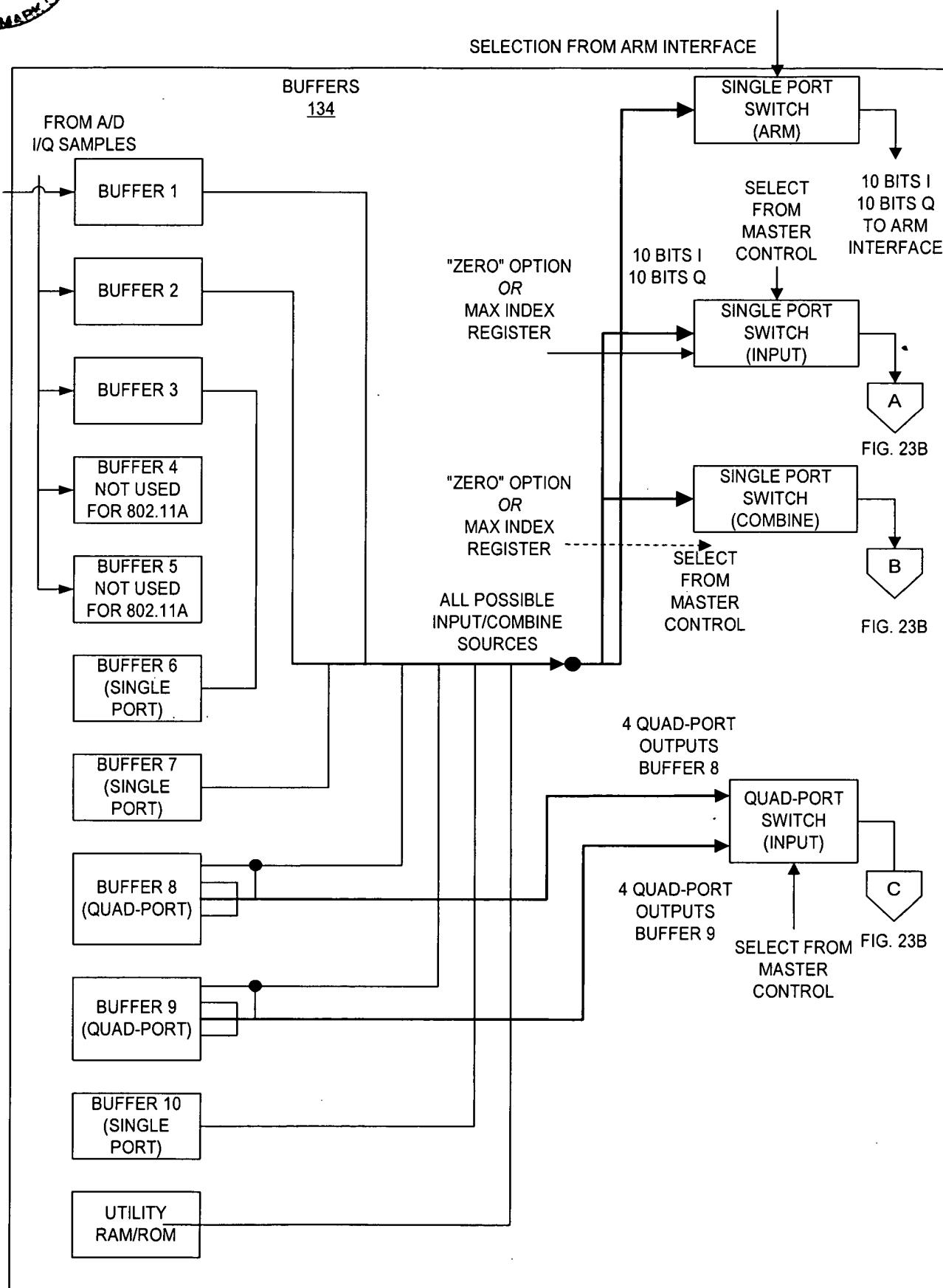


FIG. 23A

FIG. 23B

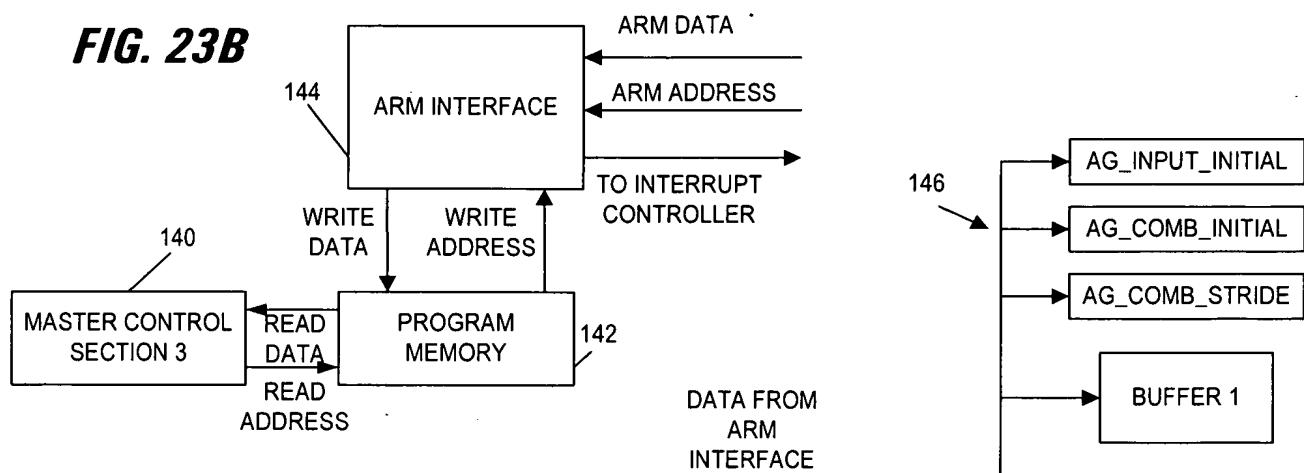
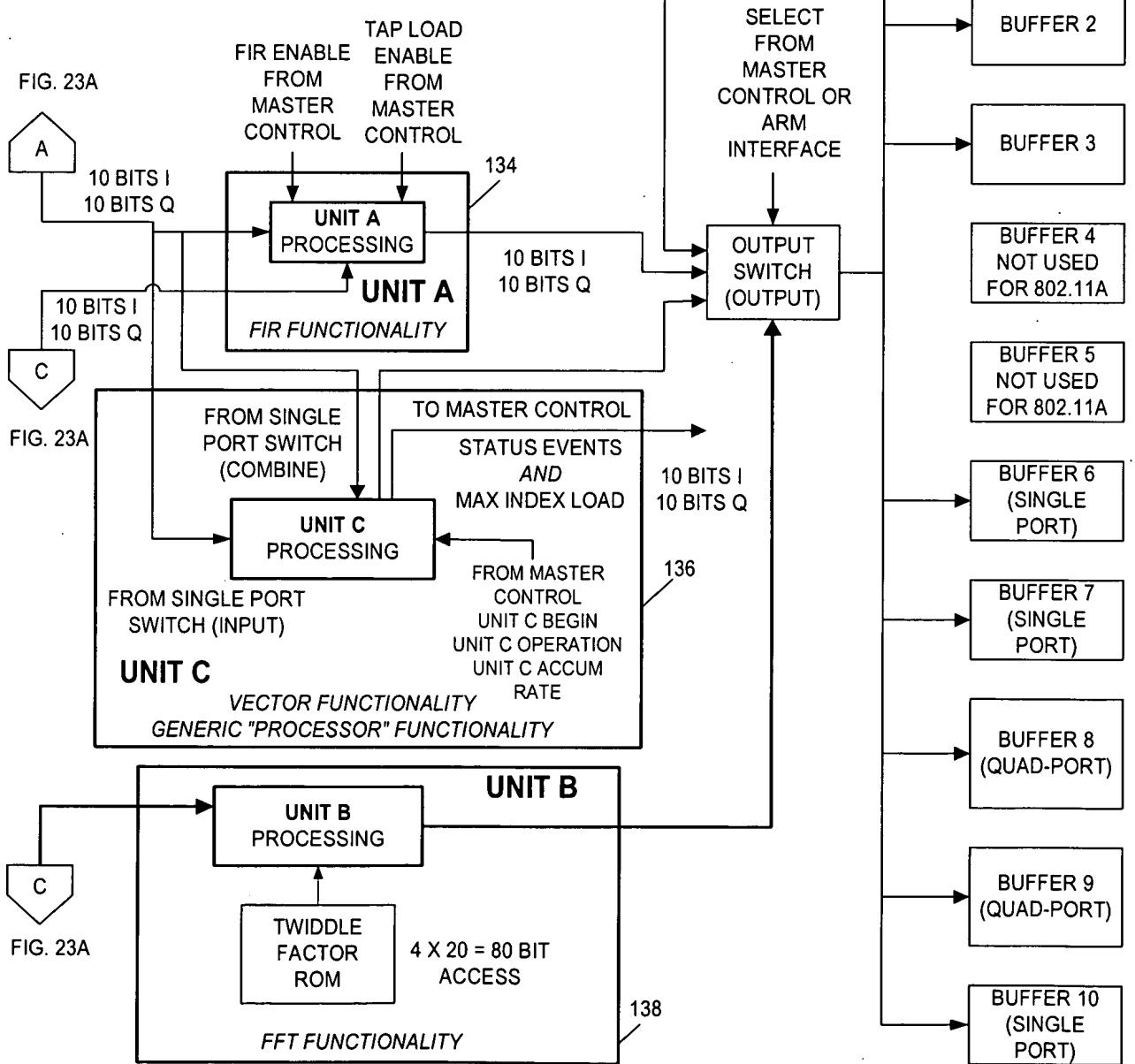


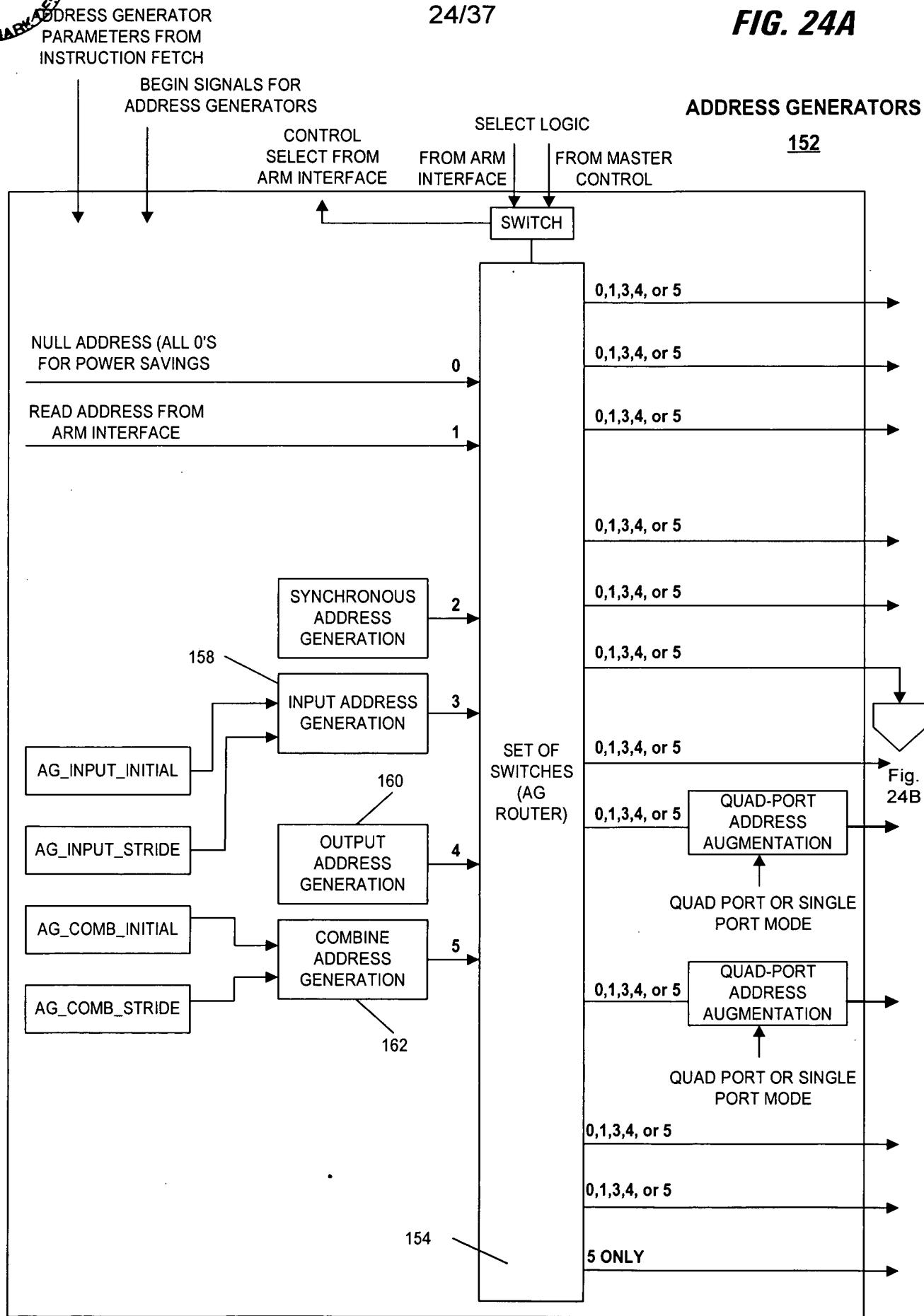
FIG. 23A

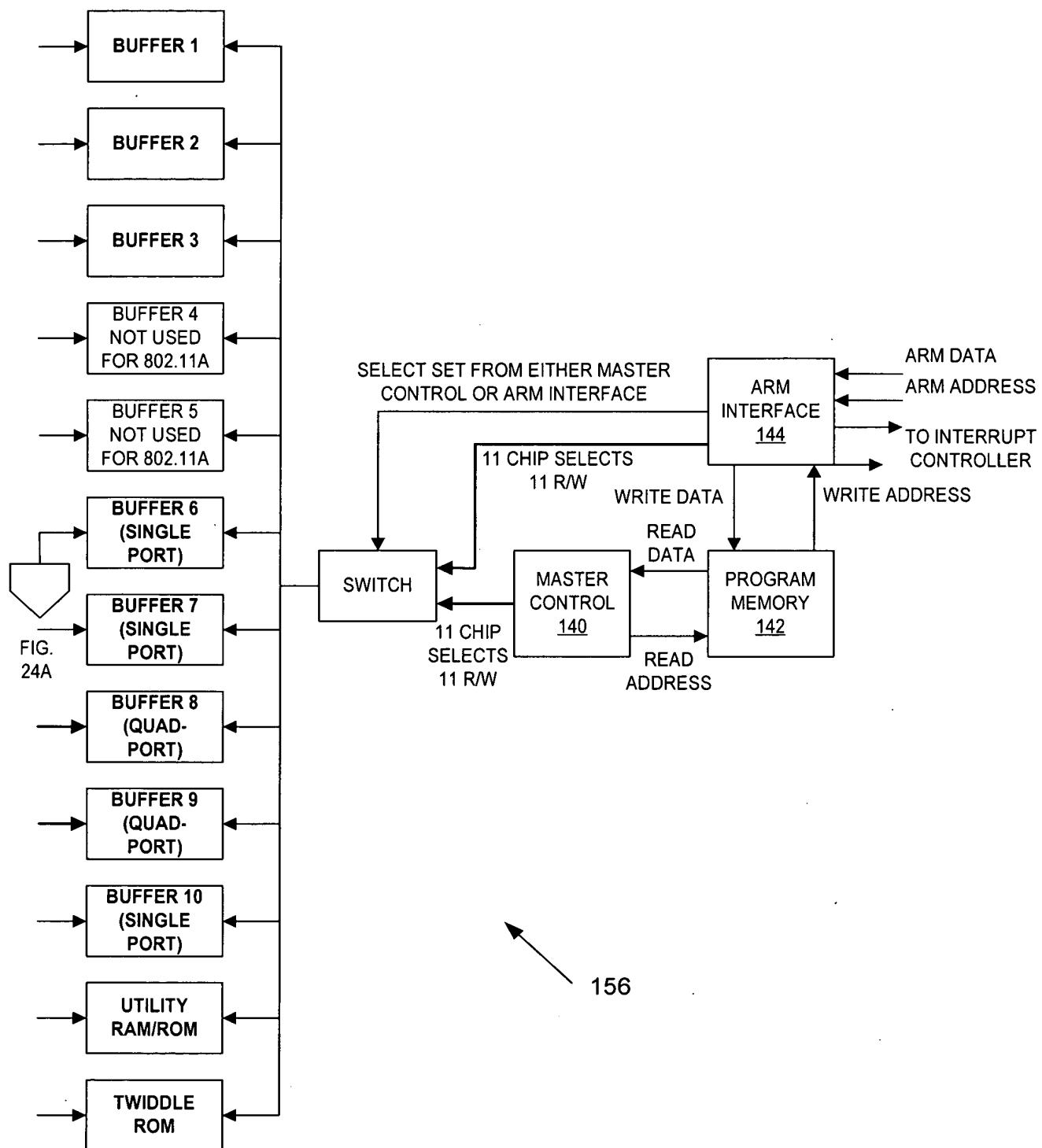




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FIG. 24A

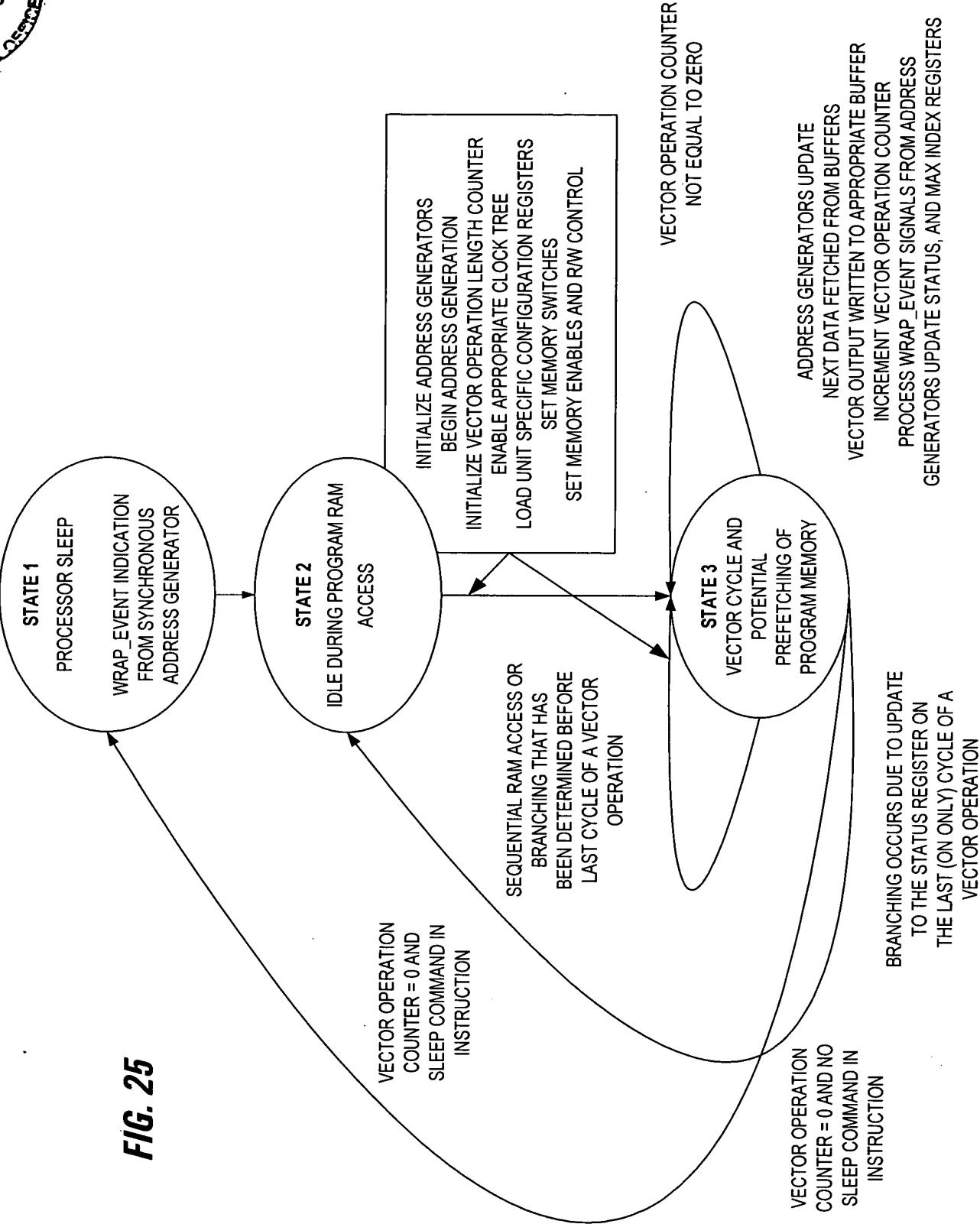


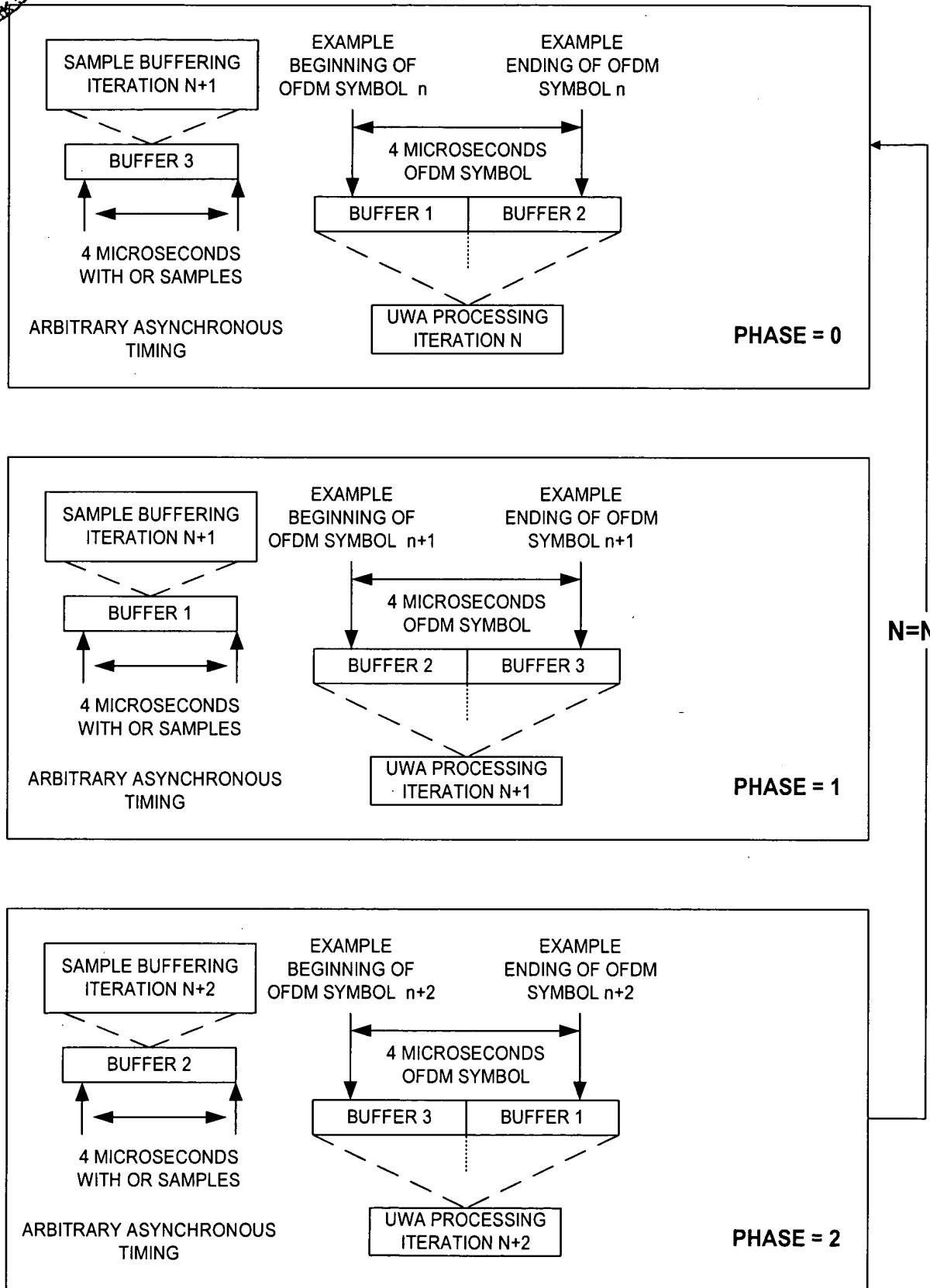
**FIG. 24B**



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FIG. 25

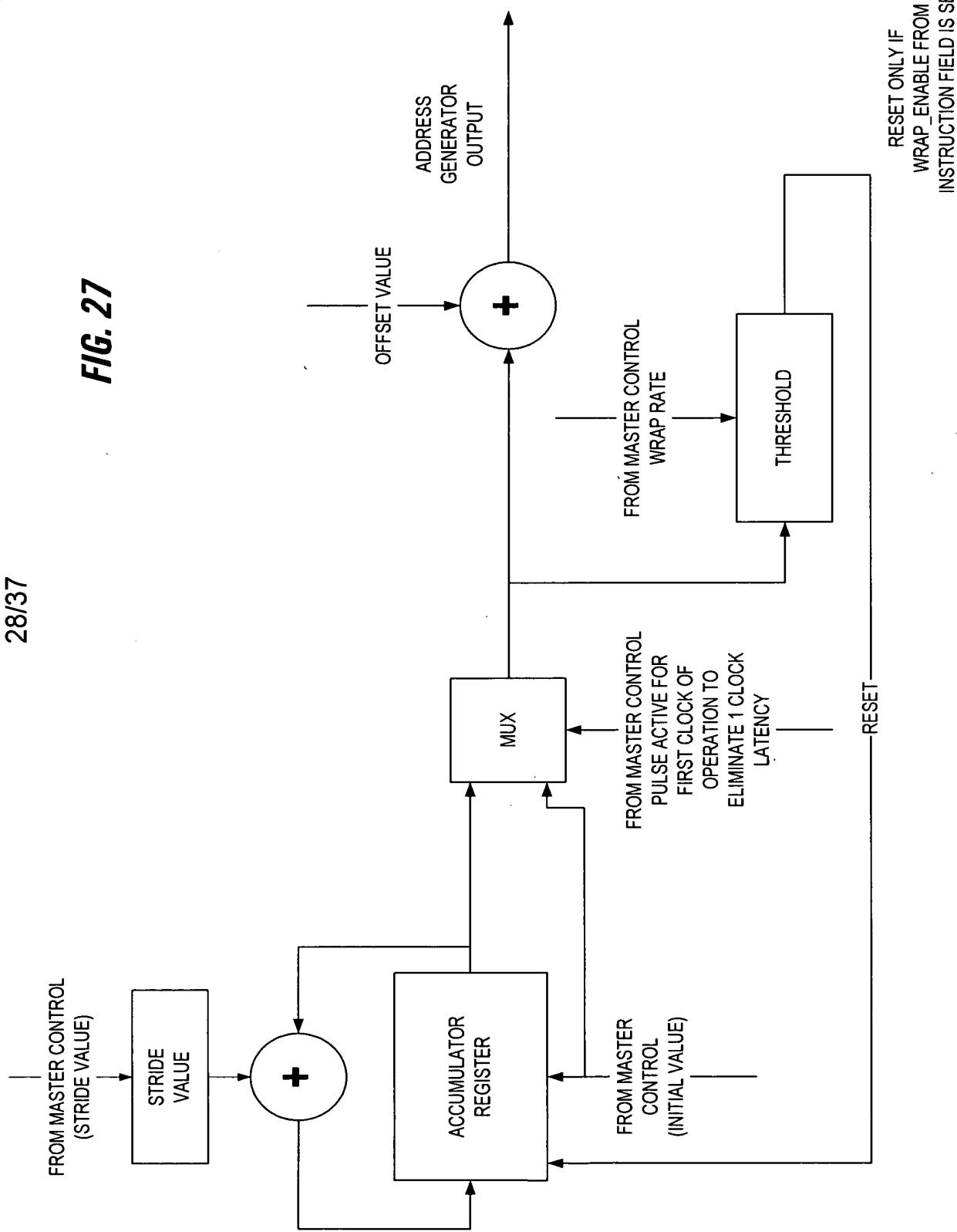


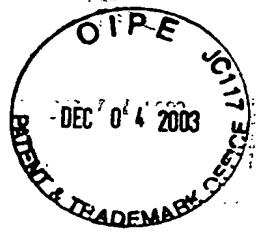
**FIG. 26**



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FIG. 27





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CLOCK UNDER
CONTROL OF VECTOR
STATE MACHINE

UNIT A

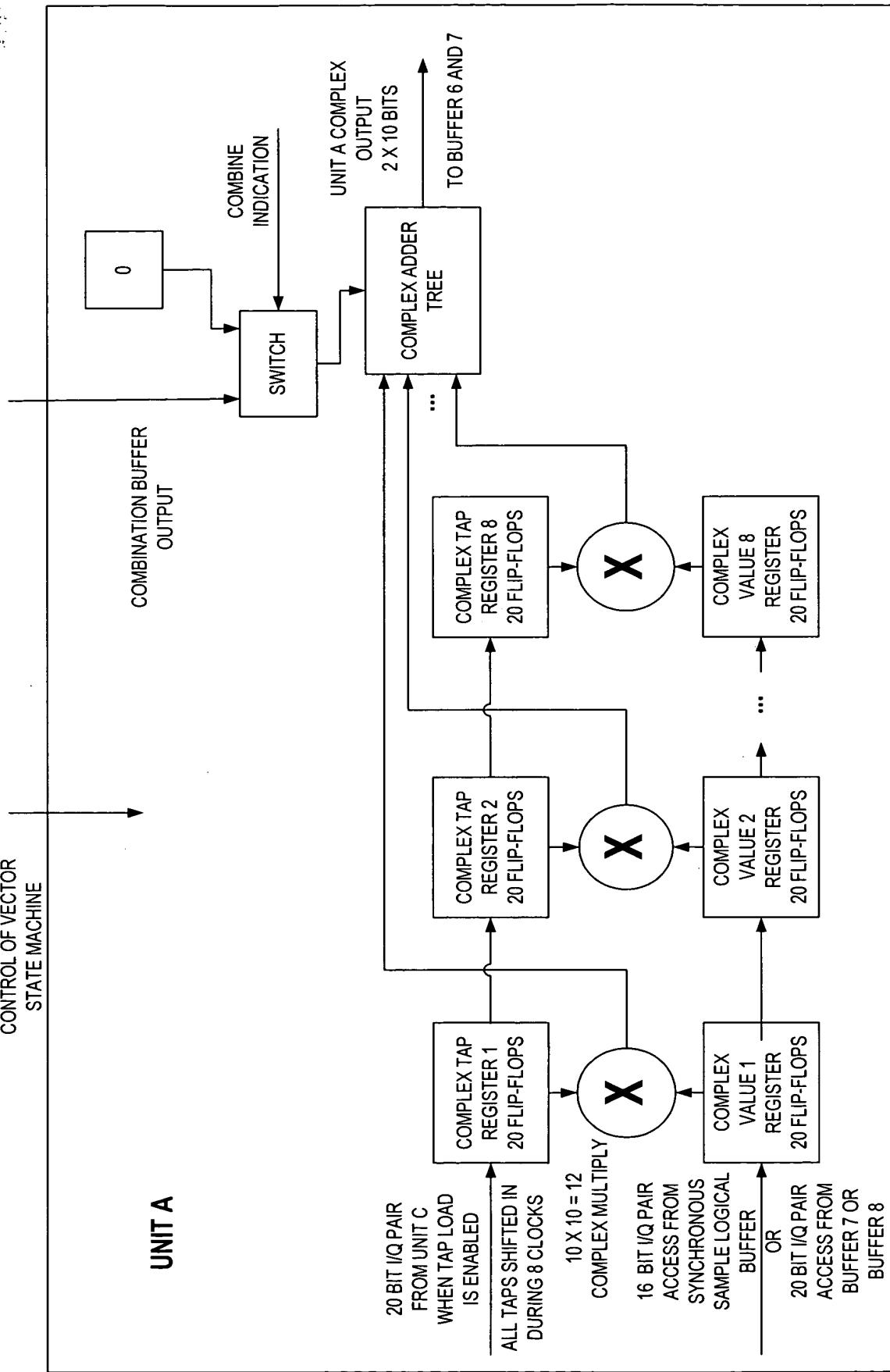


FIG. 28

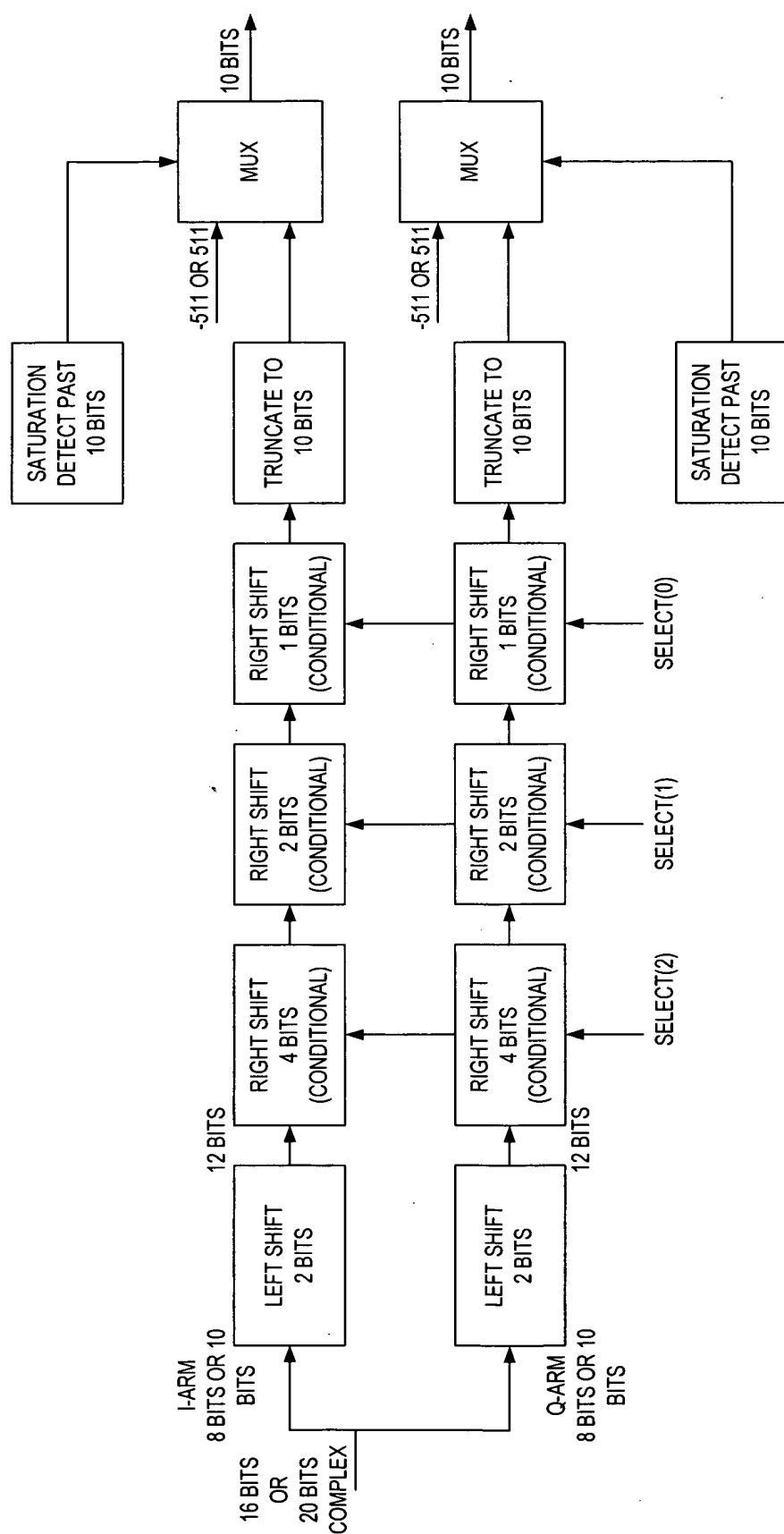


FIG. 29



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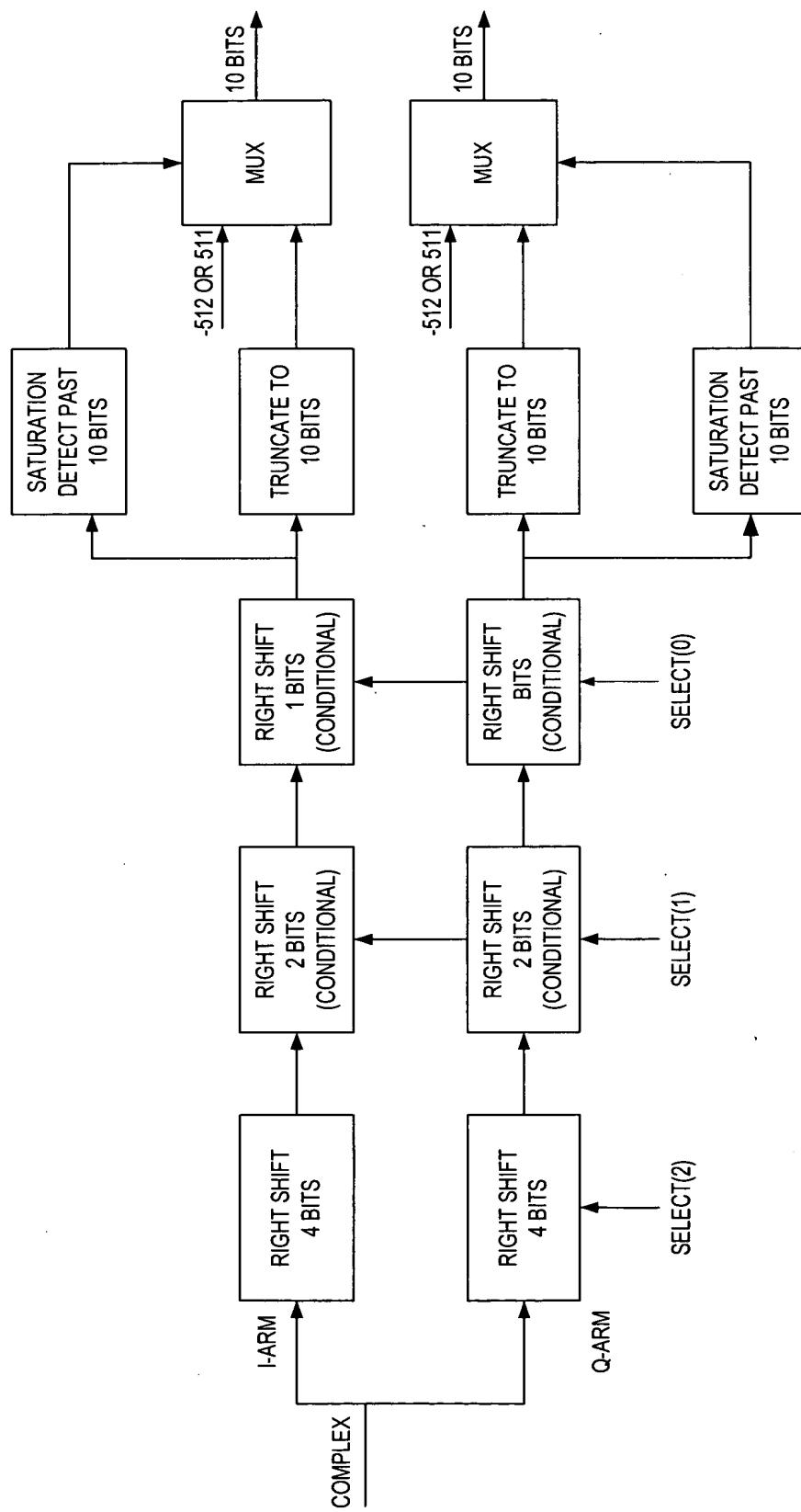
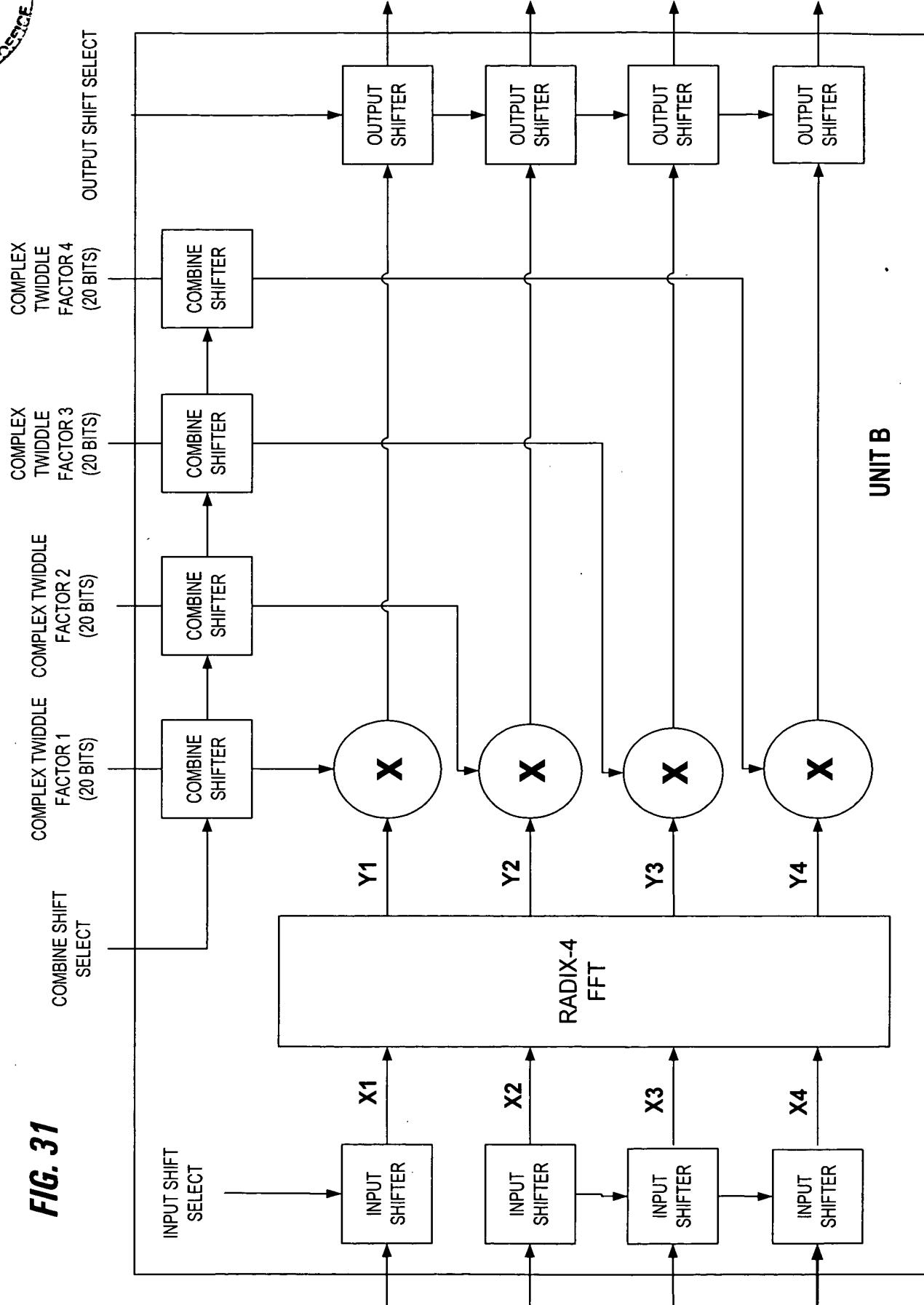


FIG. 30

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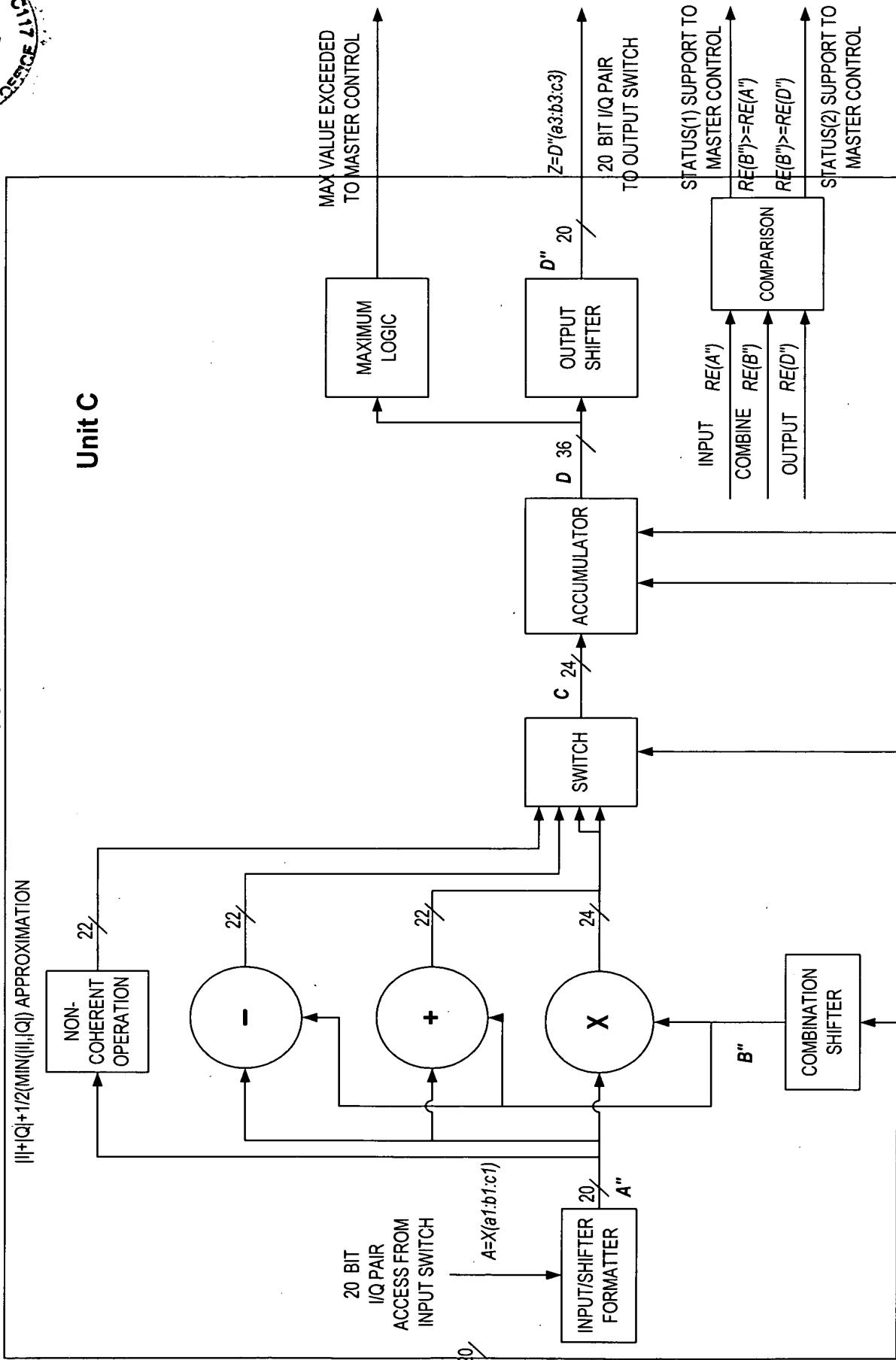
FIG. 31

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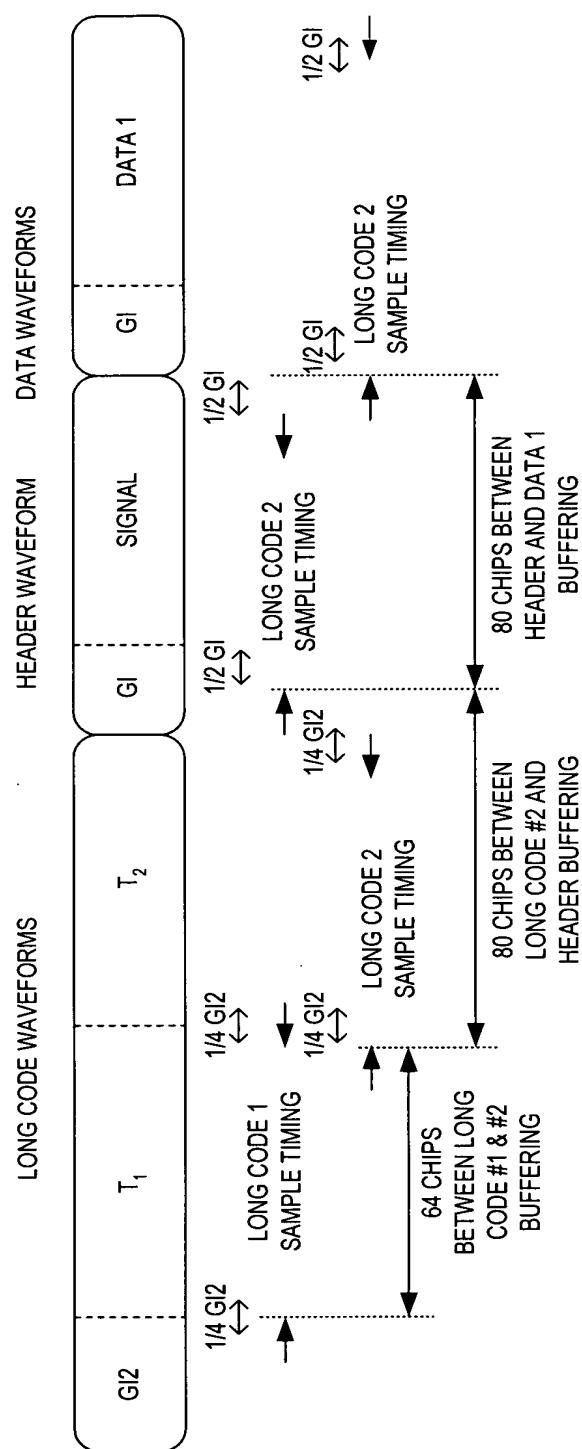


FIG. 33



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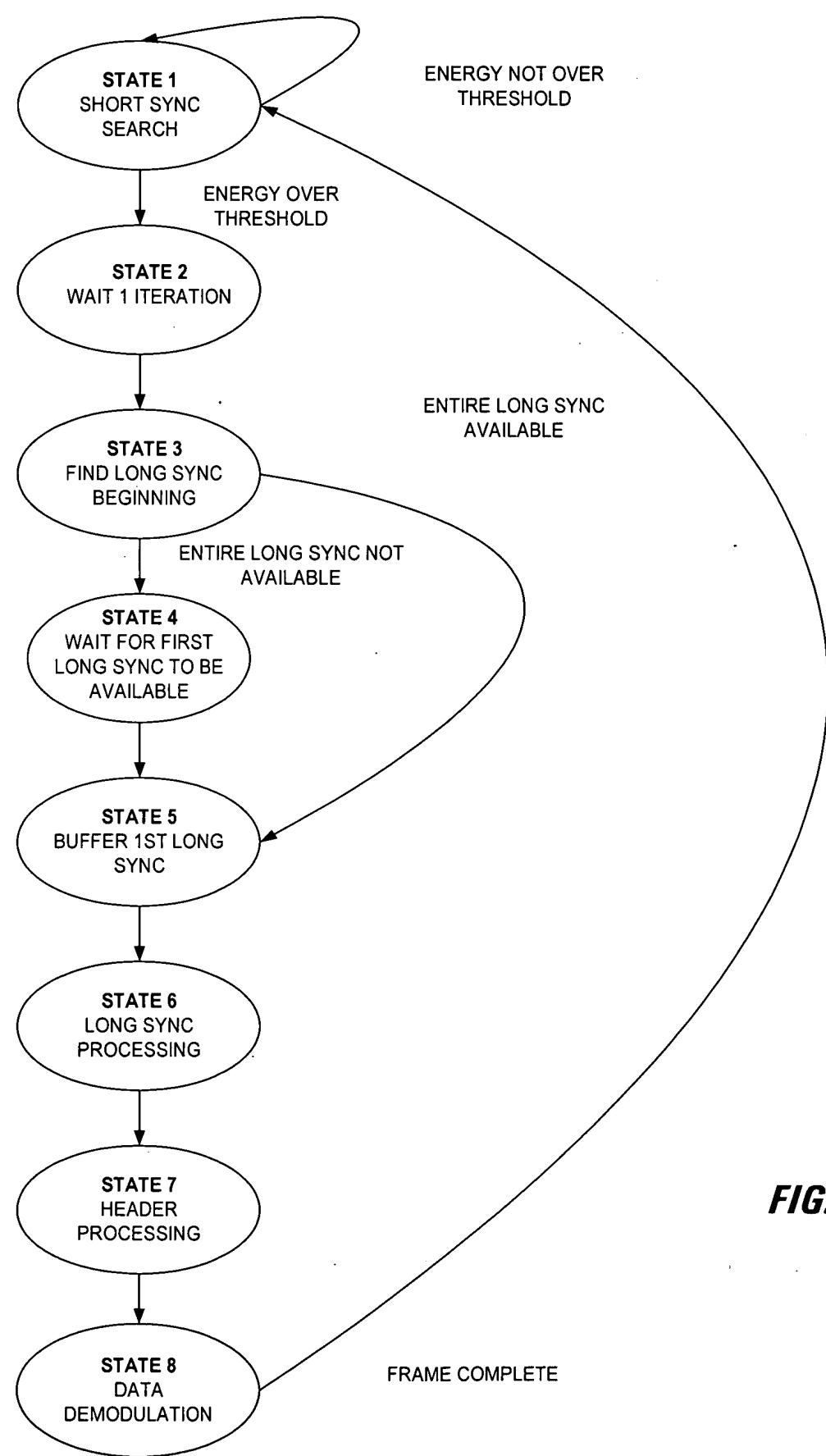


FIG. 34



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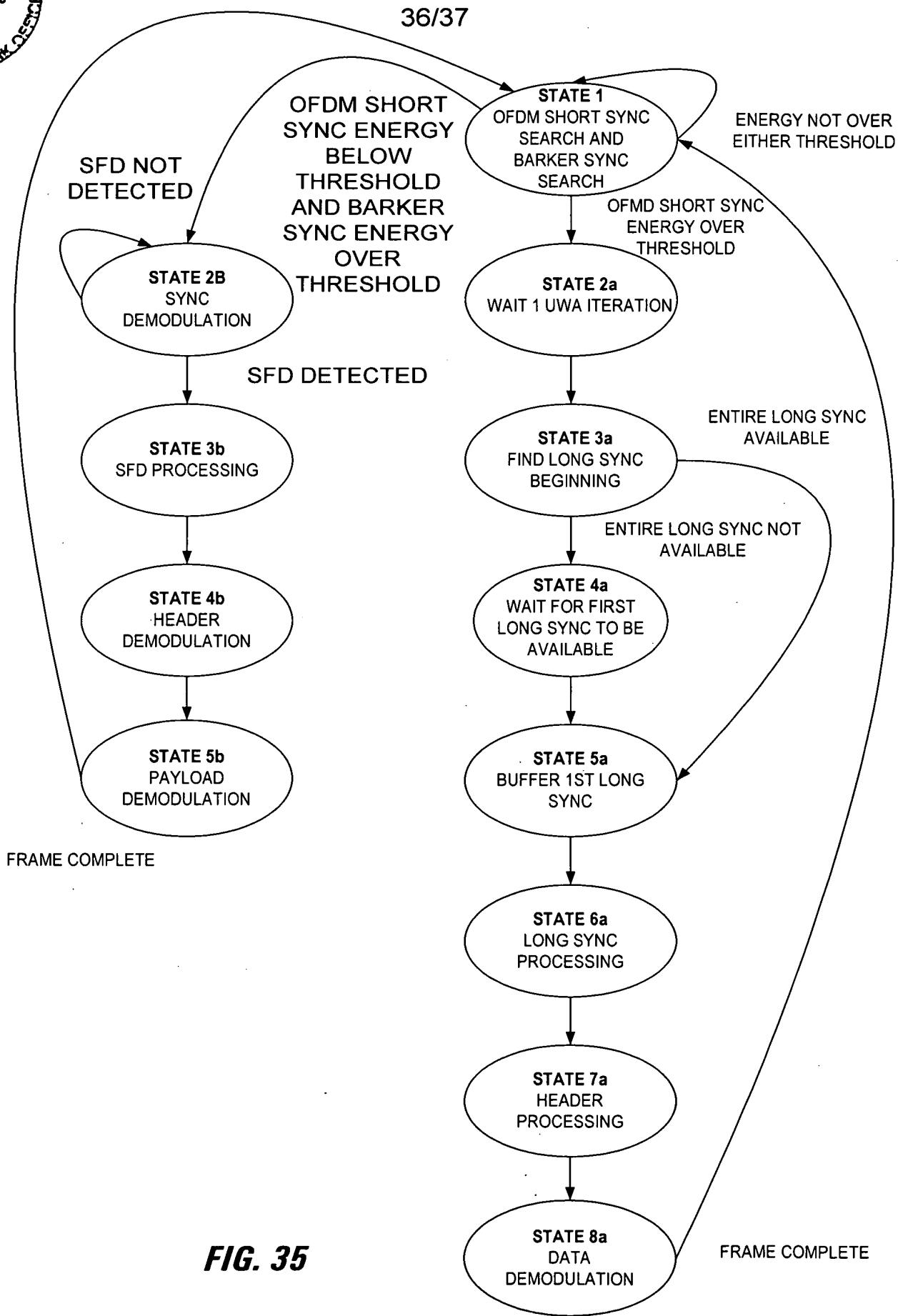


FIG. 35



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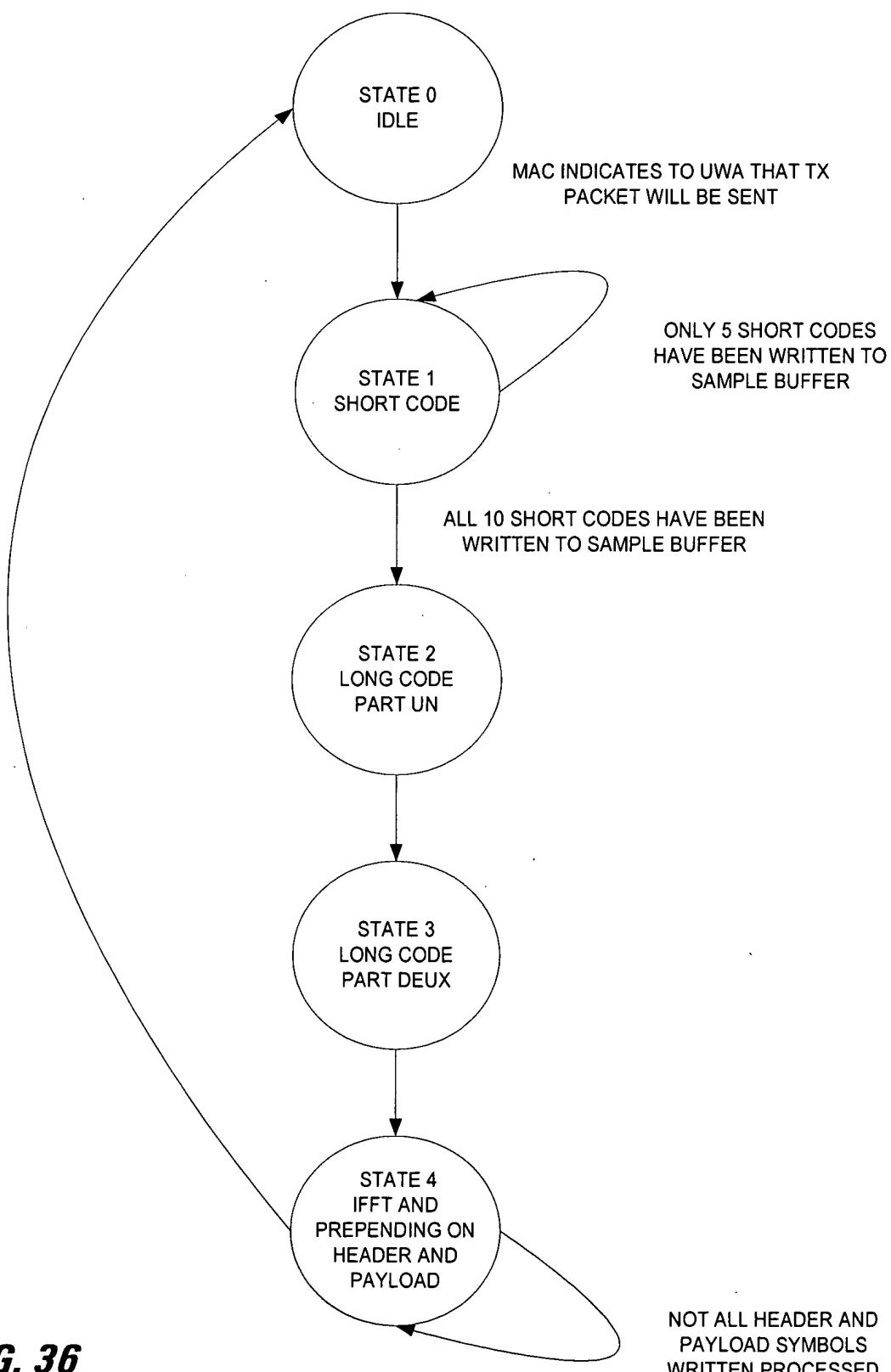


FIG. 36